

1. Assembly

- recall the packaging hierarchy: electronic systems consist of several layers of packaging, each with distinctive types of interconnection devices:

Level 0: gate-to-gate interconnections on the chip

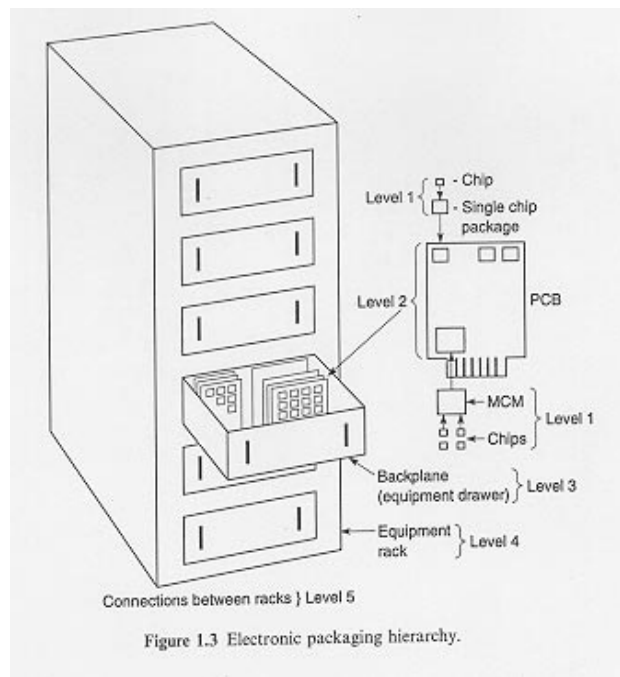
Level 1: chip-to-module connections

Level 2: board level interconnections

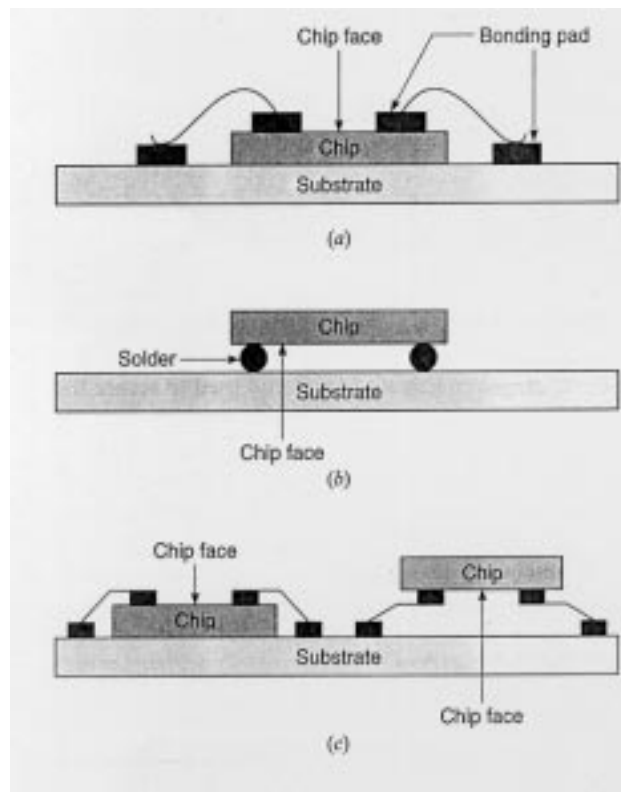
Level 3: board-to-board interconnections

Level 4: connections between sub-assemblies

Level 5: connections between systems (i.e., computer to printer)



- this course has concentrated on *Level 2*; the follow-on “Module Assembly” course focuses on *Level 1*
- ICs must be mounted on a substrate by a die attach material which permits heat conduction and ensures mechanical stability
- 3 types of die attach materials:
 - 1) solder (for eutectic bonding)
 - 2) metal-filled polymers (epoxies)
 - 3) metal-filled glasses
- methods of achieving chip-to-module connections:
 - (a) wire bonding
 - (b) flip chip bonding
 - (c) tape automated bonding (TAB)



- wire bonding = oldest method, but still the most popular for < 200 I/O's
 - involves connecting gold or aluminum wires between chip bonding pads and the package
 - time consuming because each wire must be attached individually
 - density is limited because:
 - 1) enough space is needed between adjacent bonding sites for the bonding tool to fit
 - 2) only so much space around the periphery of the chip
- flip chip requires the chip to be mounted upside down onto a carrier, module or PWB
 - electrical connections are solder bumps on surface of chip
 - density only limited by minimum distance between adjacent bonding pads
 - interconnect distance between package and chip is minimized
- TAB = developed in 1970s
 - often used with chip carriers or PWBs
 - ICs mounted onto flexible tape (usually polyimide) containing flat Cu interconnect patterns
 - pads on IC aligned to tape and bonded using thermocompression bonding
 - limitation: TAB tapes have to be custom matched to a particular chip and/or package

2. Thermal Management

- one of the key purposes of electronic packages is to cool the IC
- thermal management for electronic systems has been the driving force behind the advancement of heat transfer theory for the past 60 years
- cooling media:
 - air
 - liquid
- types of cooling:
 - immersion
 - augmented boiling
 - heat pipes
 - thermoelectric coolers
 - microchannel
 - microjet
- heat sources:
 - I^2R losses in wiring and chips
 - power supply
- most heat is generated within 25 μm of the top surface
- time averaged heat generation ranges up to ~ 2 W; instantaneous heat generation levels can reach 30-40 W
- resulting heat flux averaged over time and chip surface varies from 5-250 W/cm^2 (solar heat flux at the equator is only 0.1 W/cm^2)
- heat generated in the chips is conducted to the substrate and transferred by conduction, convection, or radiation to the surface of the package
- significant resistance to heat flow is presented by the bonding material between the chip and substrate, the substrate itself, and the thermal conducting path to the exterior surface of the package or the PWB upon which the package is mounted
- heat flux on the PWB is usually around 0.2 W/cm^2 or less
- objectives of thermal management:
 - 1) prevent catastrophic thermal failure
 - 2) extend the useful lifetime of the electronic system
- catastrophic thermal failure is usually the result of thermal fracture of a mechanical element (case or substrate) or separation of leads; can also result in semiconductor material failure due to overheating
- failure rate increases exponentially with operating temperature

EXAMPLE:

For silicon transistors, failure rate increases by a factor of 5-7 as operating temperature is raised from 25-130 °C.

- therefore, temperatures of critical components must be minimized to increase reliability and lifetime
- thermal stress is introduced when material with different CTEs are subjected to cycling
=> temperature cycling above +/- 15 °C around an average operating point also reduces reliability
- simplest and cheapest cooling method is natural air cooling, but this can only remove 0.05 W/cm² for a chip-to air temperature difference of 100 °C
- adding a fan can achieve up to 1 W/cm² for the same temperature difference
- other approaches:
 - immersion cooling in refrigerants with natural convection: 1 W/cm² @ 30 °C
 - immersion cooling in boiling refrigerants: 5 W/cm² @ 10 °C
 - forced convection with water: 10 W/cm² @ 50 °C

3. Reliability Considerations

- as increased density has made packages capable of performing at higher and higher levels, smaller features have become more delicate and more susceptible to failures due to corrosion, mechanical stress, or electrical overload
- reliability considerations:
 - failure mechanisms
 - probability of failure
 - accelerated life testing
 - reliability enhancement
- fortunately, failure modes for packaged ICs are very well known
- tasks for reliability engineers:
 - 1) determine which failure modes apply to a given part
 - 2) determine how probable it is for these modes to occur in field usage
 - 3) determine how to prevent these failures during the design and manufacturing phase
- components (“parts”) to consider:
 - circuit elements - transistors, capacitors, resistors, inductors, diodes
 - signal components on ICs - interconnect, vias, bondpads
 - 1st level connections - bond wires, tab leads, flip chip bonds
 - 2nd level connections - leads and pins
 - signal components on boards - metal traces
 - 3rd level connections

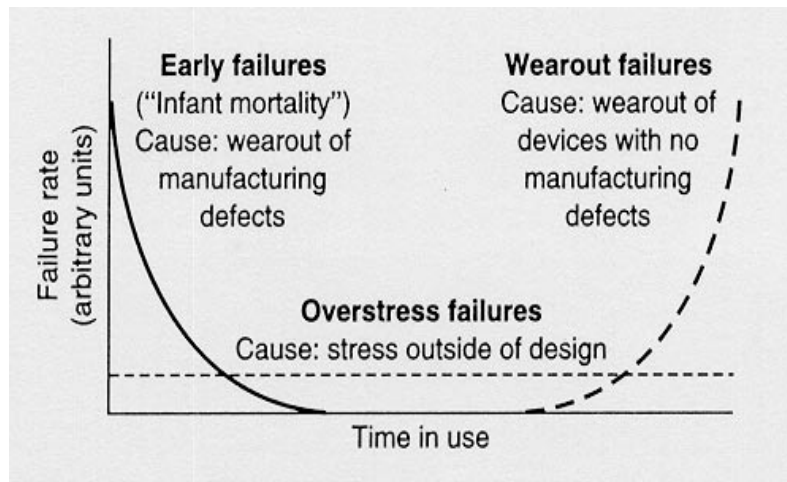
- reliability definitions:
 - 1) probability that a component will be operational within acceptable limits for a given period of time
 - 2) fraction of a group of components manufactured together that will be operational within acceptable limits for a given period of time

- quantitative definition:

$$R(8 \text{ years}) = 0.90$$

=> the reliability (i.e., probability of functionality) of a part after years of operation is 90%

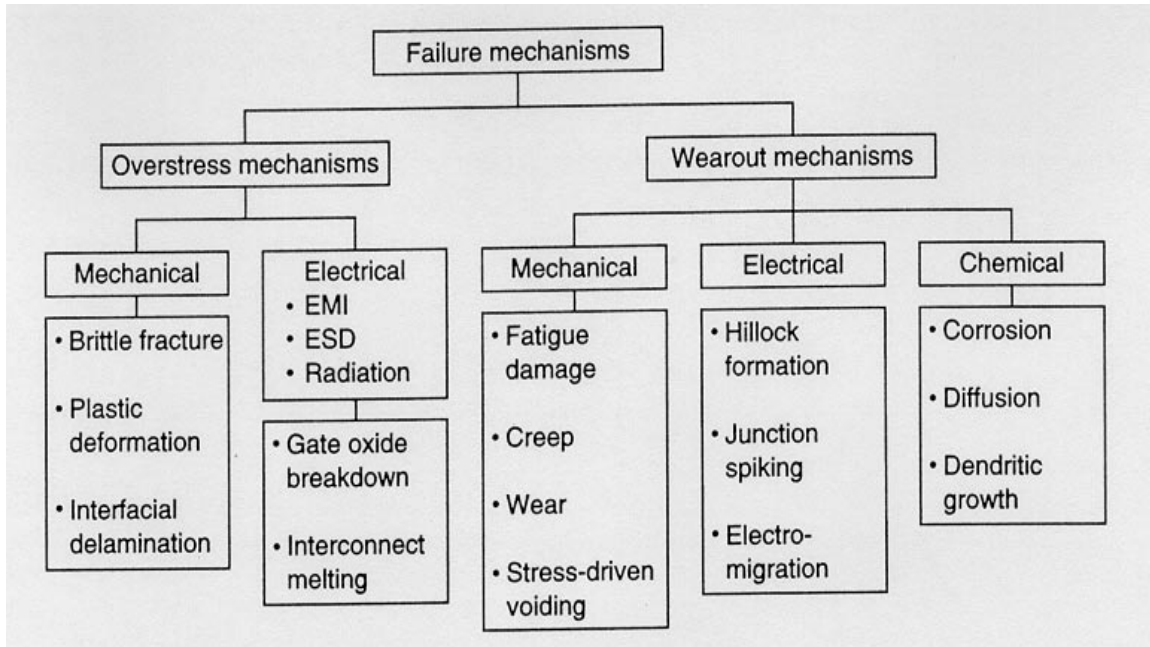
- *burn-in*: operational test in which parts are subjected to a moderate amount of thermal stress (60-90 °C for 2-24 hours) at the factory prior to final testing
- failure rate for a population of devices (“bathtub” curve):



- three components:
 - 1) early failures (“infant mortality”) - out-of-spec parts that quickly fail due to normal stress
 - 2) overstress failures (“intrinsic failures”) - caused by high-level stress beyond normal usage
 - 3) wearout failures - normal wearout at expected lifetime
- from an economic point-of-view, reliability is driven by two requirements:
 - 1) cost - device must last long enough to maximize manufacturer’s profit
 - 2) performance - safety requirements, ease of replacement
- how to estimate reliability:
 - 1) identify failure mechanisms
 - 2) perform accelerated life testing
 - 3) measure reliability
 - 4) collect failure statistics

4. Failure Mechanisms

- taxonomy of failure mechanisms in microelectronics packaging:



- failure is caused by some sort of stress: electrical, chemical, or mechanical
 - 1) overstress - stress from a single event is sufficient to cause failure
 - 2) wearout - lower level of stress over an extended period of time
- 99.9% of all failure mechanisms were identified over a decade ago
- major research effort today is not in discovering new mechanisms, but in failure prediction and prevention
- failure analysis tools:
 - optical microscopes
 - electron microscopes
 - surface analysis (Auger, XPS, SIMS, EDX)
 - package opening
 - x-ray analysis
- corrosion - most prevalent mechanism since polymers have non-zero moisture uptake
 - ☞ Consists of:
 - anodic reactions - oxidation reactions in which a metal loses electrons
 - cathodic reactions - reduction reactions in which the lost electrons combine with another species
 - ☞ Depends on:
 - thermodynamic stability of the metal
 - Au - most stable of metals relevant to packaging

Al - least stable

- availability of moisture
- presence of reducible species (like H₂)
- condition of oxide layer

👉 Prevention techniques:

- cleanliness of manufacturing environment
- monitoring of contamination levels
- cleaning parts prior to encapsulation

- electromigration - tendency of Al wires carrying large current densities ($\sim 10^6$ A/cm²) to develop opens

👉 results from “electron wind” that pushes the metal along (electrons colliding with Al atoms and transferring momentum to them)

👉 rate of metal movement described by:

$$R = AJe^{-E_a/kT}$$

where: R = flux of metal moved by electrons in g/cm²

A = constant

J = current density in A/cm²

E_a = activation energy (0.4 - 1.5 eV)

👉 Prevention techniques:

- adding 2% copper to Al wiring
- control of Al deposition parameters to decrease grain boundaries
- covering Al with tungsten
- maintaining lower current densities

- bond failures - these occur either:

1) at the bond interface

2) at the point where the bond wire joins the ball

- interconnect stress cracking - stress-induced cracks in wires

- electrostatic discharge (ESD) - static electricity

👉 can amount to over 10,000 V (enough to melt an interconnect)

👉 Prevention techniques:

- raising ambient humidity
- increasing surface electrical conductivity
- grounding all personnel

- mechanical stress - fatigue failure caused by initiation and growth of cracks due to stress