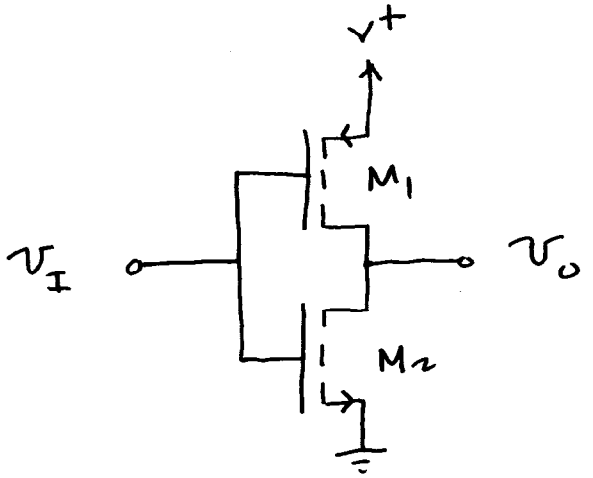
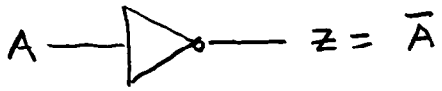
CMOS Logic Gates

The Inverter





A	Z
0	1
1	0

Assume $V_{TO} < V^+$ for M_1 and M_2

$v_I = V^+ \Rightarrow v_{GS1} = V^+ > V_{TO}$

$v_{SG2} = 0 < V_{TO}$

$\Rightarrow$ M_1 is ON

M_2 is OFF

$\Rightarrow v_O = 0$

$v_I = 0 \Rightarrow v_{SG2} = V^+ > V_{TO}$

$v_{GS1} = 0$

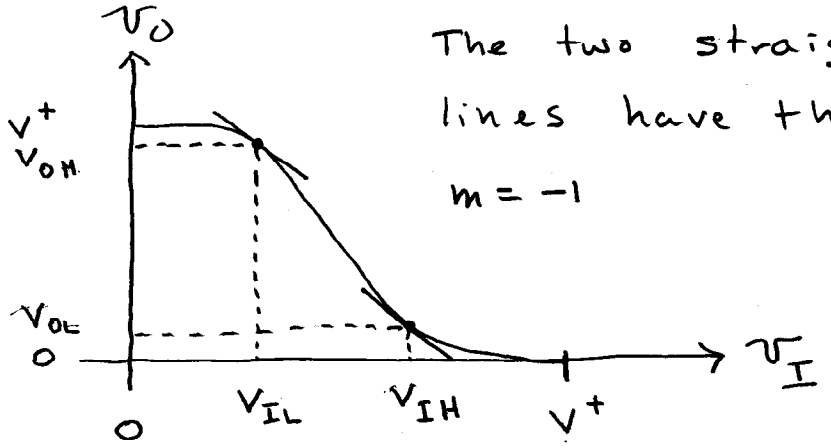
$\Rightarrow$ M_1 is OFF

M_2 is ON

Let L = 0 V. and H = V^+. The gate performs the following operations:

$$v_I = L \qquad v_o = H$$
$$v_I = H \qquad v_o = L$$

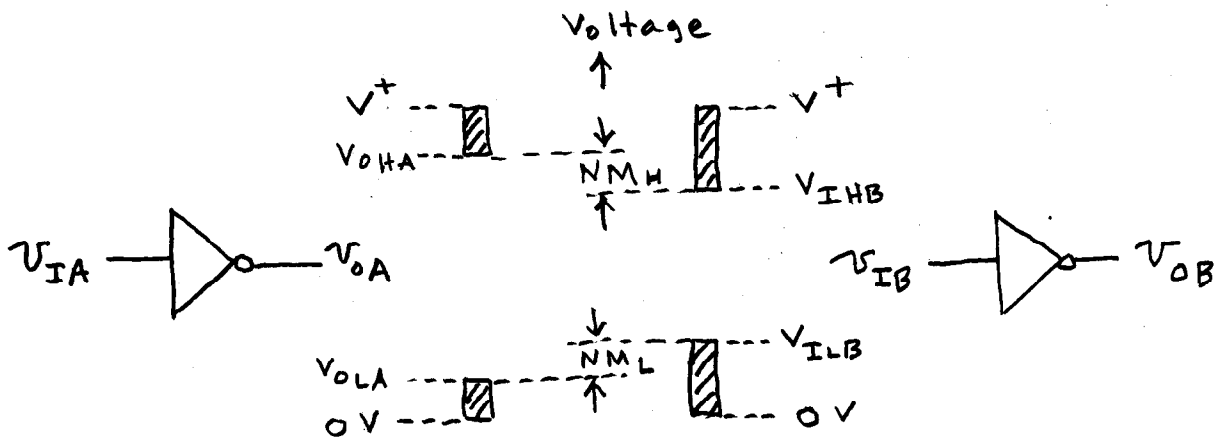
We can plot v_o versus v_I as follows:



The two straight lines have the slope $m = -1$

The noise margin is defined in terms of the voltages V_{IL}, V_{IH}, V_{OL}, and V_{OH}. The noise margins are figures of merit which relate to the susceptibility of the gate being switched by undesirable

noise at its input. To see how they are defined, consider the following circuit:



Let V_{OA} be connected to V_{IA}.
If $V_{OA} = L$, $V_{OB} = H$ if $V_{OLA} < V_{ILB}$.
We define the low noise margin as

$$NM_L = V_{ILB} - V_{OLA}$$

For identical gates, this becomes

$$NM_L = V_{IL} - V_{OL}$$

If $V_{OA} = H$, $V_{OB} = L$ if $V_{OLA} < V_{IHB}$.
We define the high noise margin

as

$$NM_H = V_{OHA} - V_{IHB}$$

For identical gates, this becomes

$$NM_H = V_{OH} - V_{IH}$$

The larger NM_L and NM_H, the more immune the gates are to false triggering by unavoidable noise voltages at its input.

If the two MOSFETs have the same value for V_{TO}, it can be shown that

$$V_{IL} = \frac{3V^+ + 2V_{TO}}{8} \qquad V_{IH} = \frac{5V^+ - 2V_{TO}}{8}$$

$$V_{OL} = \frac{V^+ - 2V_{TO}}{8} \qquad V_{OH} = \frac{7V^+ + 2V_{TO}}{8}$$

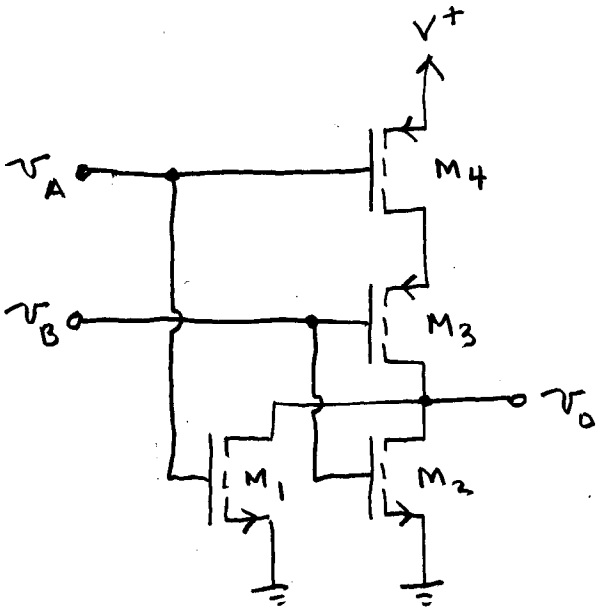
These equations give

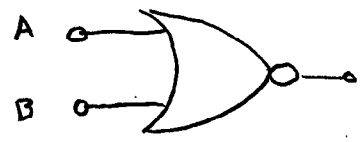
$$NM_L = NM_H = \frac{V^+ + 2V_{TO}}{4}$$

In practice, $V_{TO} \leq \frac{1}{2}V^+$. For $V_{TO} = \frac{1}{2}V^+$, we have

$$NM_L = NM_H = \frac{1}{2}V^+$$

The CMOS NOR Gate





$$Z = \overline{A+B}$$

$$= \overline{A} \cdot \overline{B}$$

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

$v_A = L \quad v_B = L$

$\Rightarrow$ M1 OFF, M2 OFF, M3 ON, and M4 ON

$\Rightarrow v_o = H$

$v_A = L \quad v_B = H$

$\Rightarrow$ M1 OFF, M2 ON, M3 OFF, and M_4 ON

$\Rightarrow v_o = L$

$v_A = H \quad v_B = L$

$\Rightarrow$ M_1 ON, M2 OFF, M3 OFF, and M4 OFF

$\Rightarrow v_o = L$

$v_A = H \quad v_B = H$

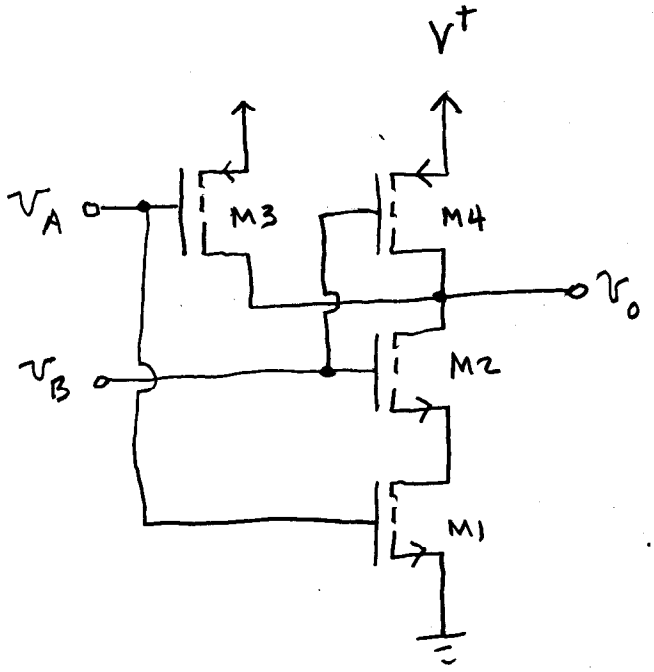
$\Rightarrow$ M1 ON, M2 ON, M3 OFF, and M4 OFF

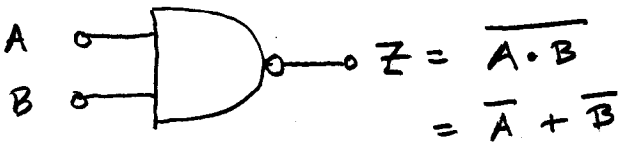
$\Rightarrow v_o = L$

v_A	v_B	v_o
L	L	H
L	H	L
H	L	L
H	H	L

This is the NOR truth table

The CMOS NAND Gate





A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

$v_A = L \quad v_B = L$

$\Rightarrow$ M1 ON, M2 OFF, M3 ON, and M4 ON

$\Rightarrow v_o = H$

$v_A = L \quad v_B = H$

$\Rightarrow$ M1 OFF, M2 ON, M3 ON, and M4 OFF

$\Rightarrow v_o = H$

$v_A = H \quad v_B = L$

$\Rightarrow$ M1 ON, M2 OFF, M3 OFF, and M4 ON

$\Rightarrow v_o = H$

$v_A = H \quad v_B = H$

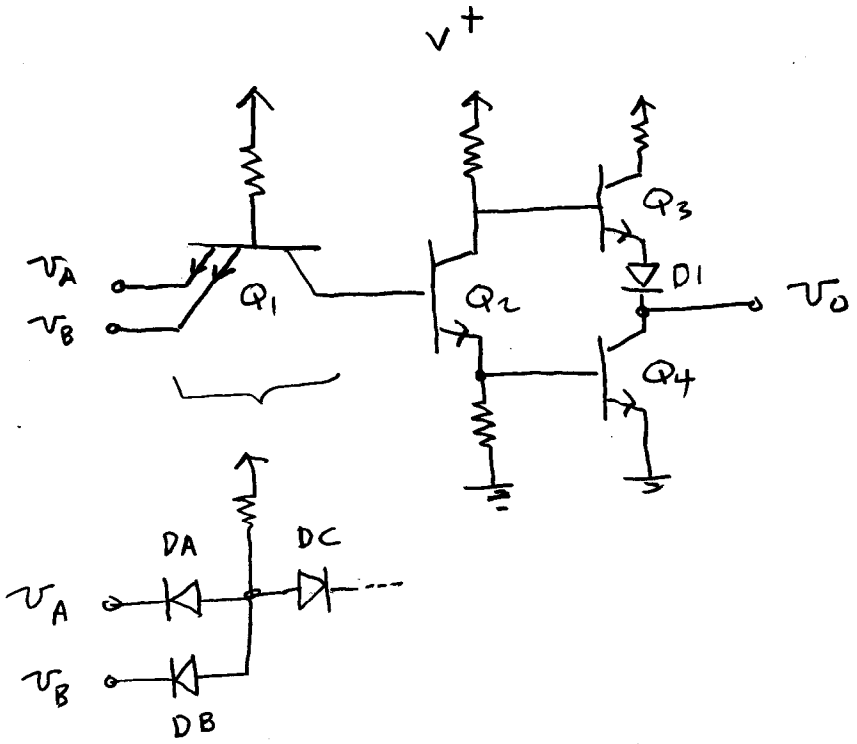
$\Rightarrow$ M1 ON, M2 ON, M3 OFF, and M_4 OFF

$\Rightarrow v_o = L$

v_A	v_B	v_o
L	L	H
L	H	H
H	L	H
H	H	L

This is the NAND truth table.

The BJT TTL NAND Gate



For $v_A = v_B = V^+$, both DA and DB are OFF. DC is turned on and a voltage is applied to the base of Q2 which saturates Q2, i.e. Q2 becomes almost a short circuit. Its emitter voltage increases, which causes Q4 to saturate. Its collector voltage decreases, which cuts off Q4. In this case $v_0 \approx 0$, i.e. $v_0 = L$.

If either $v_A = 0$ or $v_B = 0$, then DC is OFF. This cuts off Q2 and Q4. The voltage applied to the base of Q3 saturates it. In this case, $v_0 \approx V^+$, i.e. $v_0 = H$.

Thus the circuit performs the NAND operation. The purpose of D1 is to keep Q3 cut off when Q2 and Q4 are saturated.