The MOSFET

Device Symbols

Whereas the JFET has a diode junction between the gate and the channel, the metal-oxide semiconductor FET or MOSFET differs primarily in that it has an oxide insulating layer separating the gate and the channel. The circuit symbols are shown in Fig. 1. Each device has gate (G), drain (D), and source (S) terminals. Four of the symbols show an additional terminal called the body (B) which is not normally used as an input or an output. It connects to the drain-source channel through a diode junction. In discrete MOSFETs, the body lead is connected internally to the source. When this is the case, it is omitted on the symbol as shown in four of the MOSFET symbols. In integrated-circuit MOSFETs, the body usually connects to a dc power supply rail which reverse biases the body-channel junction. In the latter case, the so-called "body effect" must be accounted for when analyzing the circuit.

Figure 1: MOSFET symbols.

Device Equations

The discussion here applies to the n-channel MOSFET. The equations apply to the p-channel device if the subscripts for the voltage between any two of the device terminals are reversed, e.g. v_{GS} becomes v_{SG}. The n-channel MOSFET is biased in the active mode or saturation region for $v_{DS} \geq v_{GS} - v_{TH}$, where v_{TH} is the threshold voltage. This voltage is negative for the depletion-mode device and positive for the enhancement-mode device. It is a function of the body-source voltage and is given by

$$v_{TH} = V_{TO} + \gamma \left[\sqrt{\phi - v_{BS}} - \sqrt{\phi} \right] \tag{1}$$

where V_{TO} is the value of v_{TH} with $v_{BS} = 0$, γ is the body threshold parameter, ϕ is the surface potential, and v_{BS} is the body-source voltage. The drain current is given by

$$i_D = \frac{k'}{2} \frac{W}{L} \left(1 + \lambda v_{DS}\right) \left(v_{GS} - v_{TH}\right)^2 \tag{2}$$

where W is the channel width, L is the channel length, λ is the channel-length modulation parameter, and k' is given by

$$k' = \mu_0 C_{ox} = \mu \frac{\epsilon_{ox}}{t_{ox}} \tag{3}$$

In this equation, μ_0 is the average carrier mobility, C_{ox} is the gate oxide capacitance per unity area, ϵ_{ox} is the permittivity of the oxide layer, and t_{ox} is its thickness. It is convenient to define a transconductance coefficient K given by

$$K = \frac{k'}{2} \frac{W}{L} \left(1 + \lambda v_{DS}\right) = K_0 \left(1 + \lambda v_{DS}\right) \tag{4}$$

where K_0 is given by

$$K_0 = \frac{k'}{2} \frac{W}{L} \tag{5}$$

With these definitions, the drain current can be written

$$i_D = K \left(v_{GS} - v_{TH}\right)^2 \tag{6}$$

Note that K plays the same role in the MOSFET drain current equation as β plays in the JFET drain current equation.

Some texts define $K = k' \left(W/L\right) \left(1 + \lambda v_{DS}\right)$ so that i_D is written $i_D = \left(K/2\right) \left(v_{GS} - v_{TH}\right)^2$. In this case, the numerical value of K is twice the value used here. To modify the equations given here to conform to this usage, replace K in any equation given here with $K/2$.

Transfer and Output Characteristics

The transfer characteristics are a plot of the drain current i_D as a function of the gate-to-source voltage v_{GS} with the drain-to-source voltage v_{DS} held constant. Fig. 2 shows the typical transfer characteristics for a zero body-to-source voltage. In this case, the threshold voltage is a constant, i.e. $v_{TH} = V_{TO}$. For $v_{GS} \leq V_{TO}$, the drain current is zero. For $v_{GS} > V_{TO}$, Eq. (6) shows that the drain current increases as the square of the gate-to-source voltage. The slope of the curve represents the small-signal transconductance g_m, which is defined in the following.
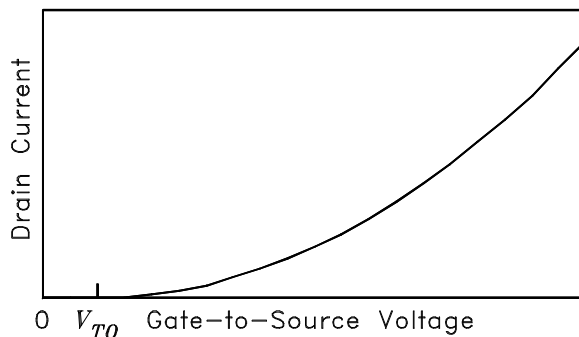

Figure 2: Drain current i_D versus gate-to-source voltage v_{GS} for constant drain-to-source voltage v_{DS}.

The output characteristics are a plot the drain current i_D as a function of the drain-to-source voltage v_{DS} with the gate-to-source voltage v_{GS} and the body-to-source voltage v_{BS} held constant. Fig. 3 shows the typical output characteristics for several values of gate-to-source voltage v_{GS}. The dashed line divides the triode region from the saturation or active region. In the saturation region, the slope of the curves represents the reciprocal of the small-signal drain-source resistance r_0, which is defined in the next section.

Small-Signal Models

There are two small-signal circuit models which are commonly used to analyze MOSFET circuits. These are the hybrid-π model and the T model. The two models are equivalent and give identical results. They are described below. In addition, a simplified small-model is derived which is called the source equivalent circuit. The models are first developed for the case of no body effect and then with the body effect. The former
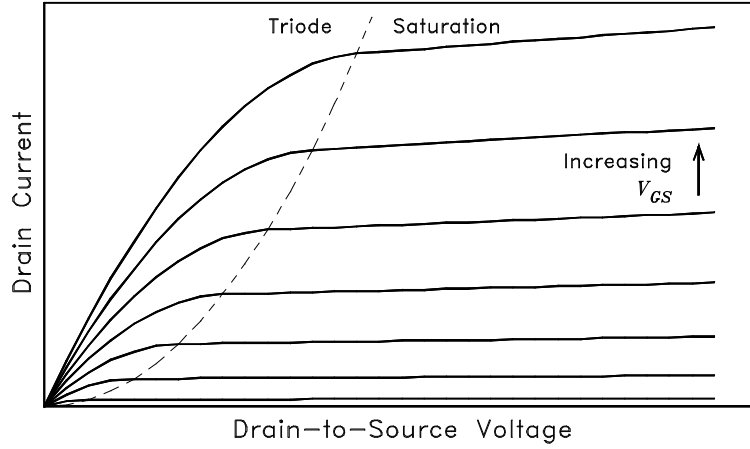
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Figure 3: Drain current i_D versus drain-to-source voltage v_{DS} for constant gate-to-source voltage v_{GS}.

case assumes that the body-source voltage is zero, i.e. $v_{BS} = 0$. This is the case with discrete MOSFETs in which the source is connected physically to the body. It also applies to small-signal ac analyses for which the body and source leads are connected to the same or different dc voltages. In this case, the small-signal body-source voltage is zero, i.e. $v_{bs} = 0$, and there is no body effect.

No Body Effect

The small-signal models in this section assume that the body lead is connected to the source lead. The models also apply when the body and source leads are connected to different dc voltages so that the ac or signal voltage from body to source is zero.

Hybrid-π Model

Consider the case where the body-source voltage is zero, i.e. $v_{BS} = 0$. In this case, the threshold voltage in Eq. 1 is a constant and given by $v_{TH} = V_{TO}$. Let the drain current and each voltage be written as the sum of a dc component and a small-signal ac component as follows:

$$i_D = I_D + i_d \tag{7}$$

$$v_{GS} = V_{GS} + v_{gs} \tag{8}$$

$$v_{DS} = V_{DS} + v_{ds} \tag{9}$$

If the ac components are sufficiently small, we can write

$$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} \tag{10}$$

where the derivatives are evaluated at the dc bias values. Let us define

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = K \left(V_{GS} - V_{TH} \right) = 2\sqrt{KI_D} \tag{11}$$

$$r_0 = \left[\frac{\partial I_D}{\partial V_{DS}} \right]^{-1} = \left[\frac{k'}{2} \frac{W}{L} \lambda \left(V_{GS} - V_{TH} \right)^2 \right]^{-1} = \frac{1/\lambda + V_{DS}}{I_D} \tag{12}$$

It follows that the small-signal drain current can be written

$$i_d = i_d' + \frac{v_{ds}}{r_0} \tag{13}$$

where
$$i'_d = g_m v_{gs} \tag{14}$$

The small-signal circuit which models these equations is given in Fig. 4(a). This is called the hybrid-π model.
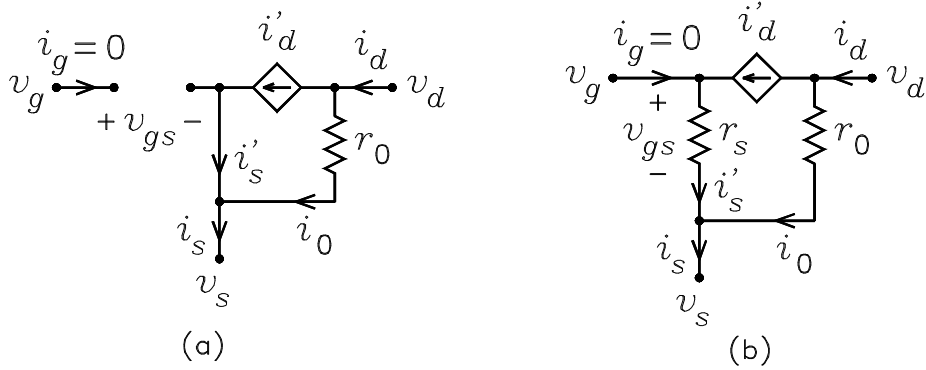

Figure 4: (a) Hybrid-π model. (b) T model.

T Model

The T model of the MOSFET is shown in Fig. 4(b). The resistor r_0 is given by Eq. (12). The resistor r_s is given by

$$r_s = \frac{1}{g_m} \tag{15}$$

where g_m is the transconductance defined in Eq. (11). The currents are given by

$$i_d = i'_s + \frac{v_{ds}}{r_0} \tag{16}$$

$$i'_s = \frac{v_{gs}}{r_s} = g_m v_{gs} \tag{17}$$

The currents in the T model are the same as for the hybrid-π model. Therefore, the two models are equivalent. Note that the gate and body currents in Fig. 4(b) are zero because the controlled source supplies the current that flows through r_s.

The Drain Equivalent Circuit

If the FET output is taken from the drain, the input can be either applied to the gate or to the source. If it is applied to the gate, the circuit is called a common-source amplifier. If it is applied to the source, the circuit is called a common-gate amplifier. In some cases, separate inputs can be applied to both the gate and the source. In any of these cases, the drain output can be solved for by first making a small-signal Thévenin or Norton equivalent circuit seen looking into the drain. We solve for the Norton equivalent circuit here. We assume that the circuits external to the gate and the source can be represented by Thévenin equivalents.

Figure 5(a) shows the FET symbol with separate Thévenin sources connected to the gate and the source. The bias circuits are not shown, but we assume that the bias solutions are known. Figure 5(b) shows the circuit with the FET replaced with the hybrid-π model.

The Norton equivalent circuit seen looking into the drain consists of a parallel current source $i_{d(sc)}$ and resistor r_{id} connecting between the drain and ground. This is shown in Figure 5(c). The value of $i_{d(sc)}$ is the drain current with $v_d = 0$, i.e. with the drain node grounded. From Figure 5(b), this current is given by

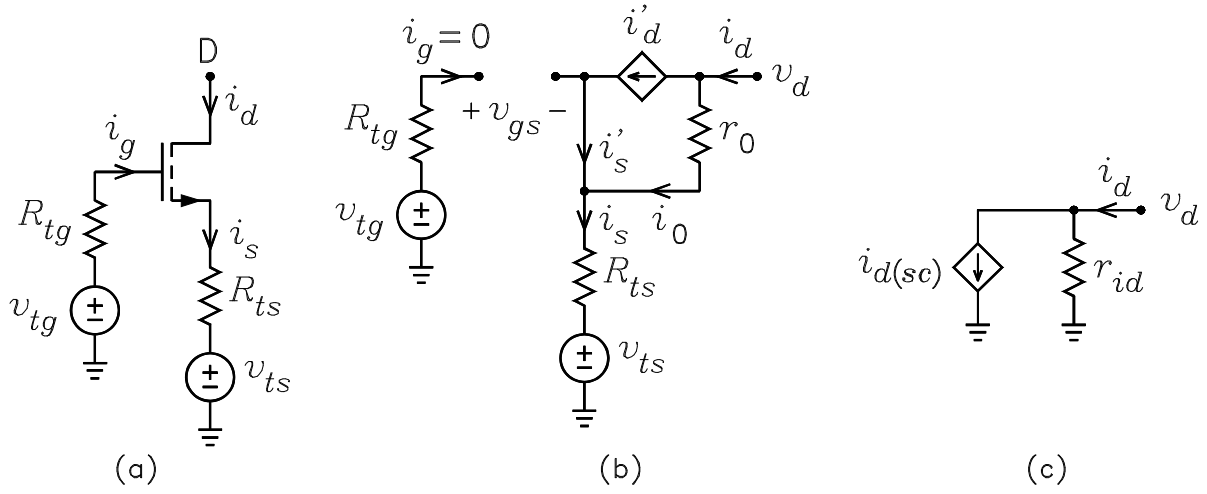$$i_{d(sc)} = i'_d + i_0 \simeq i'_d \tag{18}$$

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Figure 5: (a) FET with Thevenin sources connected to the gate and the source. (b) Circuit with the FET replaced with its hybrid-π model. (c) Drain Norton equivalent circuit.

where the approximation assumes that the current i_0 through r_0 is small compared to i'_d. This is usually a very good approximation because r_0 is a large value resistor. We call it the "r_0 approximation" when the current i_0 is neglected. In many cases, r_0 is taken to be an infinite resistor, in which case the approximation is exact.

To solve for i'_d, we can write the loop equation

$$
\begin{aligned}
v_{tg} - v_{ts} &= v_{gs} + i_s R_{ts} \\
&= v_{gs} + (i'_s + i_0) R_{ts} \\
&= \frac{i'_d}{g_m} + (i'_d + i_0) R_{ts} \\
&\simeq i'_d \left(\frac{1}{g_m} + R_{ts} \right)
\end{aligned}
\tag{19}
$$

where the relations $v_{gs} = i'_d/g_m$ and $i'_s = i'_d$ have been used. It follows that we can write

$$
i_{d(sc)} = i'_d = G_m \left(v_{tg} - v_{ts} \right)
\tag{20}
$$

where G_m is an equivalent transconductance given by

$$
G_m = \frac{1}{\dfrac{1}{g_m} + R_{ts}} \overset{\text{or}}{=} \frac{1}{r_s + R_{ts}}
\tag{21}
$$

where $r_s = 1/g_m$.

We next solve for the resistance r_{id} seen looking into the drain node. Consider the drain current i_d to be an independent current source and set $v_{tg} = v_{ts} = 0$. We can write

$$
\begin{aligned}
v_d &= i_0 r_0 + i_s R_{ts} \\
&= (i_d - i'_d) r_0 + i_s R_{ts} \\
&= i_d (r_0 + R_{ts}) - i'_d r_0
\end{aligned}
\tag{22}
$$

$$
i'_d = g_m v_{gs} = -g_m v_s = -g_m i_s R_{ts} = -g_m i_d R_{ts}
\tag{23}
$$

where $v_{gs} = -v_s$ and $i_s = i_d$ have been used. Substitution of i'_d from the second equation into the first equation yields

$$
\begin{aligned}
v_d &= i_d (r_0 + R_{ts}) + g_m i_d R_{ts} r_0 \\
&= i_d \left[r_0 (1 + g_m R_{ts}) + R_{ts} \right]
\end{aligned}
\tag{24}
$$

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It follows that the drain resistance is given by

$$r_{id} = \frac{v_d}{i_d} = r_0\left(1 + g_m R_{ts}\right) + R_{ts} \stackrel{\text{or}}{=} r_0\left(1 + \frac{R_{ts}}{r_s}\right) + R_{ts} \tag{25}$$

Note that no approximations have been made in solving for r_{id}.

In summary, the small-signal Norton equivalent circuit seen looking into the drain of a FET is a current source $i_{d(sc)}$ in parallel with a resistor r_{id} given by

$$i_{d(sc)} = i'_d = G_m\left(v_{tg} - v_{ts}\right) \tag{26}$$

$$G_m = \frac{1}{\dfrac{1}{g_m} + R_{ts}} \stackrel{\text{or}}{=} \frac{1}{r_s + R_{ts}} \tag{27}$$

$$r_{id} = r_0\left(1 + g_m R_{ts}\right) + R_{ts} \stackrel{\text{or}}{=} r_0\left(1 + \frac{R_{ts}}{r_s}\right) + R_{ts} \tag{28}$$

where v_{tg} and v_{ts}, respectively, are the Thévenin voltages seen looking out of the gate and source and R_{ts} is the Thévenin resistance in series with v_{ts}. Note that R_{tg} does not appear in the equations because the current through it is zero.

Example 1 *Figure 6(a) shows the signal equivalent circuit of a common-source amplifier. It is given that $R_{tg} = 1\,\text{k}\Omega$, $R_{ts} = 50\,\Omega$, $R_D = 10\,\text{k}\Omega$, $I_D = 1\,\text{mA}$, $K = 1.5\,\text{mA/V}^2$, and $r_0 = 50\,\text{k}\Omega$. Solve for the voltage gain and output resistance of the circuit.*
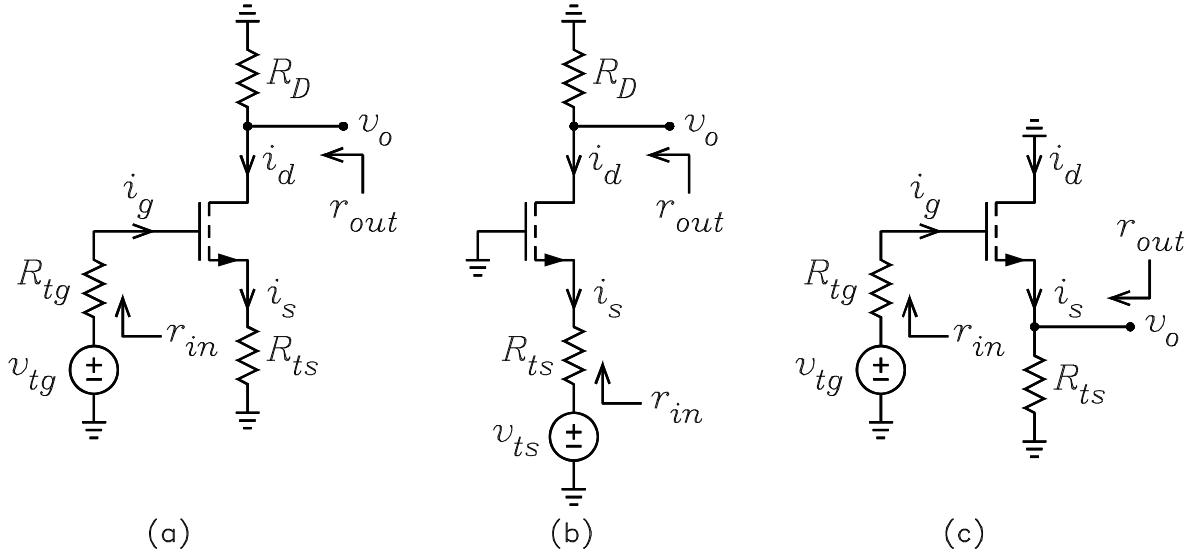

Figure 6: (a) Common-source amplifier. (b) Common-gate amplifier. (c) Common-drain amplifier.

Solution: $g_m = 2\sqrt{K I_D} = 2.45\,\text{mS}$, $r_s = 1/g_m = 408\,\Omega$.

A flow graph for the voltage gain is shown in Figure 7(a). From the flow graph, we can write

$$\frac{v_o}{v_{tg}} = \frac{i'_d}{v_{tg}} \times \frac{v_o}{i'_d} = G_m \times -\left(r_{id}\|R_D\right) \tag{29}$$

The numerical values are

$$G_m = \frac{1}{r_s + R_{ts}} = \frac{1}{458} \tag{30}$$

$$r_{id} = r_0\left(1 + \frac{R_{ts}}{r_s}\right) + R_{ts}$$

$$= 50\mathrm{k}\left(1 + \frac{50}{408}\right) + 50 = 56.2\,\mathrm{k\Omega} \tag{31}$$

$$\frac{v_o}{v_{tg}} = G_m \times -(r_{id}\|R_C) = \frac{1}{458} \times -\frac{56.2\mathrm{k} \times 10\mathrm{k}}{56.2\mathrm{k} + 10\mathrm{k}} = -18.5 \tag{32}$$

$$r_{out} = r_{id}\|R_D = \frac{56.2\mathrm{k} \times 10\mathrm{k}}{56.2\mathrm{k} + 10\mathrm{k}} = 8.49\,\mathrm{k\Omega} \tag{33}$$

Because the gain is negative, the amplifier is said to be an inverting amplifier.

$$v_{tg} \xrightarrow{\;G_m\;i_d'\;} \bullet \xrightarrow{\;-r_{id}\|R_{td}\;} \bullet\, v_o \qquad\qquad v_{ts} \xrightarrow{\;-G_m\;i_d'\;} \bullet \xrightarrow{\;-r_{id}\|R_{td}\;} \bullet\, v_o$$

$$\text{(a)} \qquad\qquad\qquad\qquad\qquad\qquad \text{(b)}$$
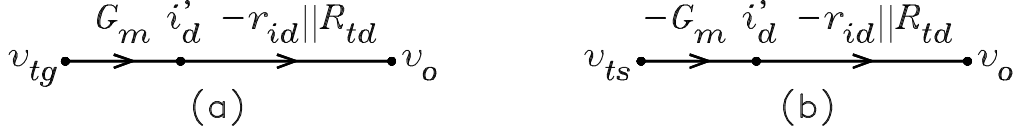
Figure 7: (a) Flow graph for the CS amplifier. (b) Flow graph for the CG amplifier.

Example 2 *Figure 6(b) shows the signal equivalent circuit of a common-gate amplifier. It is given that $R_{ts} = 50\,\Omega$, $R_D = 10\,\mathrm{k\Omega}$, $I_D = 1\,\mathrm{mA}$, $K = 1.5\,\mathrm{mA/V^2}$, and $r_0 = 50\,\mathrm{k\Omega}$. Solve for the voltage gain and output resistance of the circuit.*

Solution: $g_m = 2\sqrt{KI_D} = 2.45\,\mathrm{mS}$, $r_s = 1/g_m = 408\,\Omega$.
    A flow graph for the voltage gain is shown in Figure 7(b). From the flow graph, we can write

$$\frac{v_o}{v_{ts}} = \frac{i_d'}{v_{ts}} \times \frac{v_o}{i_d'} = -G_m \times -(r_{id}\|R_C)$$

The numerical values are

$$G_m = \frac{1}{r_s + R_{ts}} = \frac{1}{408 + 50} = \frac{1}{458}$$

$$r_{id} = r_0\left(1 + \frac{R_{ts}}{r_s}\right) + R_{ts}$$

$$= 50\mathrm{k}\left(1 + \frac{50}{408}\right) + 50 = 56.2\,\mathrm{k\Omega}$$

$$\frac{v_o}{v_{tg}} = -G_m \times -(r_{id}\|R_C) = \frac{1}{458} \times \frac{56.2\mathrm{k} \times 10\mathrm{k}}{56.2\mathrm{k} + 10\mathrm{k}} = 18.5$$

$$r_{out} = r_{id}\|R_D = \frac{56.2\mathrm{k} \times 10\mathrm{k}}{56.2\mathrm{k} + 10\mathrm{k}} = 8.49\,\mathrm{k\Omega}$$

Because the gain is positive, the amplifier is said to be a non-inverting amplifier.

The Gate Equivalent Circuit

Because the gate current $i_g = 0$, the equivalent circuit seen looking into the gate is an open circuit.
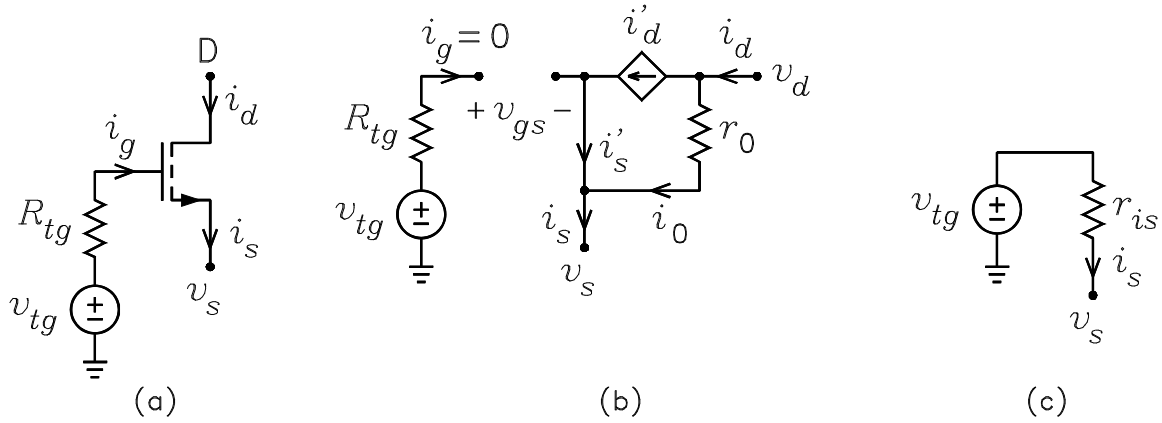
Figure 8: (a) BJT symbol with a Thévenin source connected to the base. (b) Circuit with the BJT replaced with its hybrid-π model. (c) Thévenin emitter equivalent circuit.

The Source Equivalent Circuit

Figure 8(a) shows the FET symbol with a Thévenin source connected to the gate. The bias circuits are not shown, but we assume that the bias solutions are known. We wish to solve for the small-signal Thévenin equivalent circuit seen looking into the source. Figure 8(b) shows the circuit with the FET replaced with the hybrid-π model.

From the circuit in 8(b), we can write

$$
\begin{aligned}
v_s &= v_{tg} - v_{gs} \\
&= v_{tg} - \frac{i'_d}{g_m} \\
&= v_{tg} - \frac{i'_s}{g_m} \\
&= v_{tg} - \frac{i_s - i_0}{g_m} \\
&\simeq v_{tg} - \frac{i_s}{g_m}
\end{aligned}
\tag{34}
$$

where the approximation assumes i_0 is small compared to i_s has been used. It follows that the Thévenin equivalent circuit seen looking into the source is the voltage source v_{tg} in series with a resistance r_{is} given by

$$
r_{is} = \frac{1}{g_m} = r_s
\tag{35}
$$

The equivalent circuit is shown in Figure 8(c). There is no R_{tg} in this solution because the current through it is zero.

With the definition of r_{is}, we can define another way of calculating $i_{d(sc)}$ in the Norton drain circuit. The current i_s in Figure 5(a) is given by

$$
i_s = \frac{v_{tg} - v_{ts}}{r_{is} + R_{ts}}
\tag{36}
$$

Because $i'_d = i'_s \simeq i_s$ and $i_{d(sc)} = i'_d = G_m (v_{tg} - v_{ts})$, we have a third equation for G_m given by

$$
G_m = \frac{1}{r_{is} + R_{ts}}
\tag{37}
$$

Example 3 *Figure 6(c) shows the signal equivalent circuit of a common-drain amplifier. It is given that $R_{tg} = 10\,\text{k}\Omega$, $R_{ts} = 1\,\text{k}\Omega$, $I_D = 1\,\text{mA}$, $K = 1.5\,\text{mA}/\text{V}^2$, and $r_0 = 50\,\text{k}\Omega$. Solve for the voltage gain and output resistance of the circuit.*

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Solution: $g_m = 2\sqrt{KI_D} = 2.45\,\mathrm{mS}$, $r_s = 1/g_m = 408\,\Omega$.

$$r_{is} = r_s = \frac{1}{g_m} = 408\,\Omega$$

$$G_m = \frac{1}{r_{is} + R_{ts}} = \frac{1}{408 + 1\mathrm{k}} = \frac{1}{1408}$$

The output resistance is

$$r_{out} = r_{is} \| R_{ts} = \frac{408 \times 1\mathrm{k}}{408 + 1\mathrm{k}} = 290\,\Omega$$

The input resistance is an open circuit.

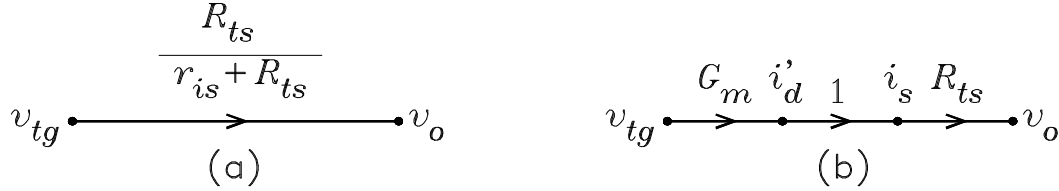Two possible flow graphs for the solution are shown in Figure 9.

Figure 9: Flow graphs for the common-collector amplifier.

The first solution for the voltage gain is illustrated in Figure 9(a), where voltage division is used to solve for the gain to obtain

$$\frac{v_o}{v_{tg}} = \frac{R_{ts}}{r_{is} + R_{ts}} = \frac{1\mathrm{k}}{408 + 1\mathrm{k}} = 0.710$$

The second solution is illustrated in Figure 9(b). The voltage gain is

$$\frac{v_o}{v_{tg}} = \frac{i'_d}{v_{tg}} \times \frac{i_s}{i'_d} \times \frac{v_o}{i_s} = G_m \times 1 \times R_{ts} = \frac{1}{1408} \times 1 \times 1\mathrm{k} = 0.710$$

Example 4 *Figure 10(a) shows a CS/CD amplifier. What are the expressions for the input resistance, the output resistance, and the voltage gain?*

Solution: Because $i_{g1} = 0$, the input resistance is an open circuit, i.e. $r_{in} = \infty$. The output resistance is

$$r_{out} = r_{is2} \| R_{S2}$$

where $r_{is2} = r_{s2} = 1/g_{m2}$. A flow graph for the voltage gain is shown in Figure 11(a). The gain is given by

$$\frac{v_o}{v_{tg}} = \frac{i'_{d1}}{v_{tg}} \times \frac{v_{tg2}}{i'_{d1}} \times \frac{v_o}{v_{tg2}} = G_{m1} \times -(r_{id1} \| R_{D1}) \times \frac{R_{S2}}{r_{is2} + R_{S2}}$$

where $G_{m1} = 1/(r_{is1} + R_{S1})$ and $r_{id1} = r_{01}(1 + g_{m1}R_{S1}) + R_{S1}$.

Example 5 *Figure 10(b) shows a combination CS amplifier and a CD/CG amplifier. What are the expressions for the input resistances, the output resistance, and the output voltage?*

Solution: Because $i_{g1} == i_{g2} = 0$, both input resistances are open circuits, i.e. $r_{in1} = r_{in2} = \infty$. The output resistance is

$$r_{out} = r_{id1} \| R_{D1}$$

where $r_{is1} = R_S + r_{is2} = R_S + 1/g_{m2}$. A flow graph for the output voltage is shown in Figure 12. It is given by

$$v_o = i'_{d1} \times r_{id1} \| R_{D1} = G_{m1} \times (v_{tg1} - v_{ts1}) \times r_{id1} \| R_{D1} = G_{m1} \times (v_{tg1} - v_{tg2}) \times r_{id1} \| R_{D1}$$
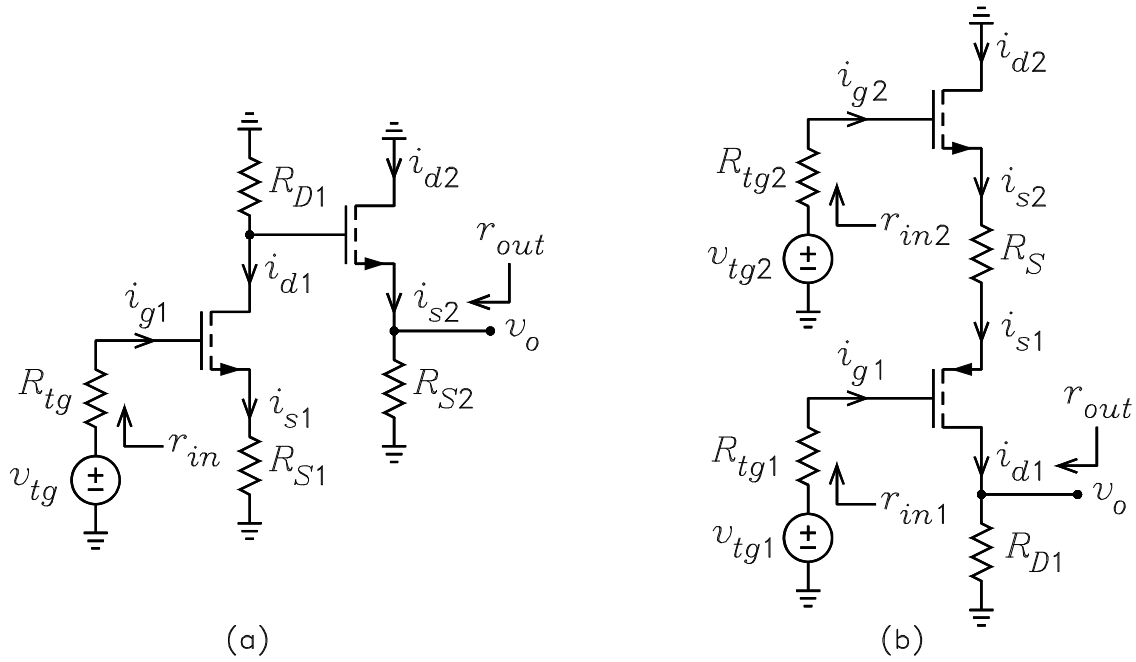
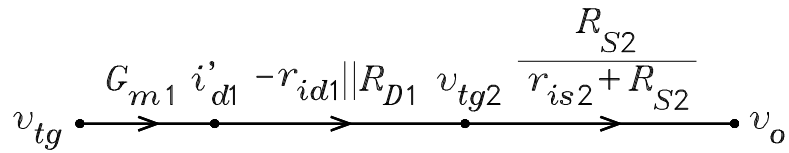Figure 10: (a) CS/CD amplifier. (b) Combination CS amplifier and CD/CG amplifier.

Figure 11: Flow graph for the CS/CD amplifier.

where

$$G_{m1} = \frac{1}{r_{is1} + R_S + r_{is2}} = \frac{1}{\dfrac{1}{g_{m1}} + R_S + \dfrac{1}{g_{m2}}}$$

$$r_{id1} = r_{01}\left[1 + g_{m1}\left(R_S + \frac{1}{g_{m2}}\right)\right] + \left(R_S + \frac{1}{g_{m2}}\right)$$
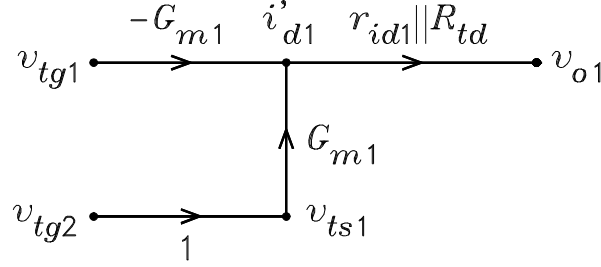

Figure 12: Flow graph for the combination CS amplifier and CD/CG amplifier.

The Body Effect

The small-signal models above assume that the body lead is connected to the source lead. In the following, we assume that the body lead is connected to ac signal ground. In integrated circuit design, this ac signal ground is typically a dc power supply rail. In this case, any ac signal voltage on the source lead causes an ac signal voltage between the body and source. The effect of this voltage is called the body effect.

Hybrid-π Model

Let the drain current and each voltage be written as the sum of a dc component and a small-signal ac component as follows:

$$i_D = I_D + i_d \tag{38}$$

$$v_{GS} = V_{GS} + v_{gs} \tag{39}$$

$$v_{BS} = V_{BS} + v_{bs} \tag{40}$$

$$v_{DS} = V_{DS} + v_{ds} \tag{41}$$

If the ac components are sufficiently small, we can write

$$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{BS}} v_{bs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} \tag{42}$$

where the derivatives are evaluated at the dc bias values. Let us define

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = K\left(V_{GS} - V_{TH}\right) = 2\sqrt{KI_D} \tag{43}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\gamma\sqrt{KI_D}}{\sqrt{\phi - V_{BS}}} = \chi g_m \tag{44}$$

$$\chi = \frac{\gamma}{2\sqrt{\phi - V_{BS}}} \tag{45}$$

$$r_0 = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1} = \left[\frac{k'}{2}\frac{W}{L}\lambda\left(V_{GS} - V_{TH}\right)^2\right]^{-1} = \frac{V_{DS} + 1/\lambda}{I_D} \tag{46}$$

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The small-signal drain current can thus be written

$$i_d = i'_d + \frac{v_{ds}}{r_0} \qquad i'_d = i_{dg} + i_{db} \tag{47}$$

where

$$i_{dg} = g_m v_{gs} \tag{48}$$

$$i_{db} = g_{mb} v_{bs} \tag{49}$$

The small-signal circuit which models these equations is given in Fig. 13(a). This is called the hybrid-π model. If the body (B) lead is connected to the source, then $v_{bs} = 0$ and the circuit becomes that given in Fig. 4(a).
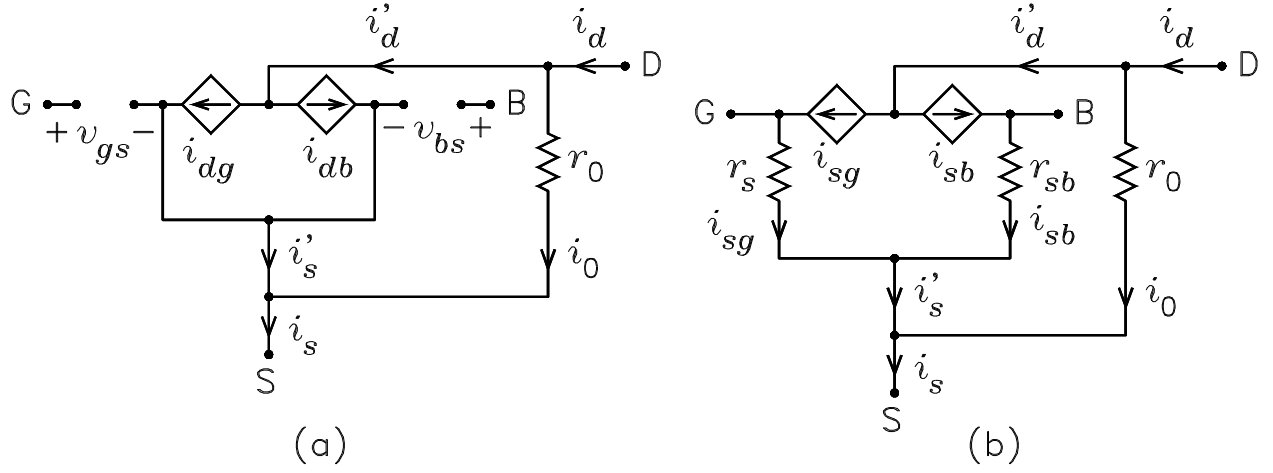

Figure 13: (a) Hybrid-π model with body effect. (b) T model with body effect.

T Model

The T model of the MOSFET is shown in Fig. 4(b). The resistor r_0 is given by Eq. (12). The resistors r_s and r_{sb} are given by

$$r_s = \frac{1}{g_m} \tag{50}$$

$$r_{sb} = \frac{1}{g_{mb}} = \frac{1}{\chi g_m} = \frac{r_s}{\chi} \tag{51}$$

where g_m and g_{mb} are the transconductances defined in Eqs. (43) and (44). The currents are given by

$$i_d = i_{sg} + i_{sb} + \frac{v_{ds}}{r_0} \tag{52}$$

$$i_{sg} = \frac{v_{gs}}{r_s} = g_m v_{gs} \tag{53}$$

$$i_{sb} = \frac{v_{bs}}{r_{sb}} = g_{mb} v_{bs} \tag{54}$$

The currents are the same as for the hybrid-π model. Therefore, the two models are equivalent. Note that the gate and body currents are zero because the two controlled sources supply the currents that flow through r_s and r_{sb}.

A Simplified T Model

There is a simplification to the T model with body effect that simplifies many calculations. Figure 14(a) shows the T model of the MOSFET with a Thévenin source connected to the gate and the body connected to signal ground. We desire the Thévenin equivalent circuit seen looking up into the i'_s branch. The open circuit or Thévenin voltage is given by

$$v_{oc} = v_{tg} \frac{r_{sb}}{r_{sg} + r_{sb}} = v_{tg} \frac{\frac{1}{g_{mb}}}{\frac{1}{g_m} + \frac{1}{g_{mb}}} = \frac{v_{tg}}{1 + \frac{g_{mb}}{g_m}} = \frac{v_{tg}}{1 + \chi} \tag{55}$$

The Thévenin resistance is calculated with $v_{tg} = 0$. Let this be denoted by r'_s. It is given by

$$r'_s = r_s \| r_{sb} = \frac{r_s r_{sb}}{r_s + r_{sb}} = \frac{r_s}{1 + \chi} \stackrel{\text{or}}{=} \frac{1}{(1 + \chi) g_m} \tag{56}$$

Figure 14(b) shows the simplified T model. For the case where the body and the source connect to the same signal node, set $\chi = 0$ in the equations.
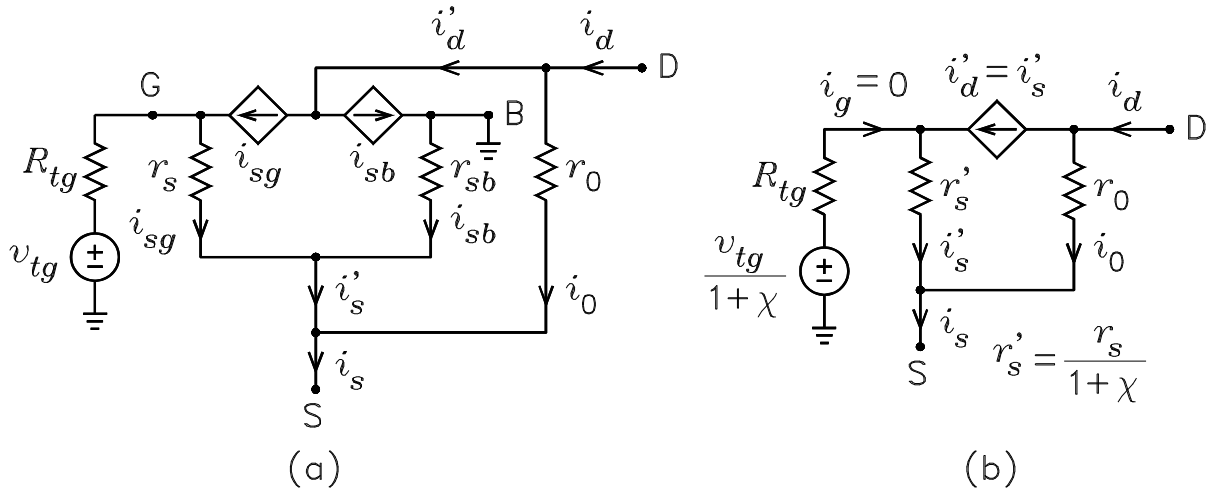

Figure 14: (a) T model with a Thévenin source connected to the gate and the body grounded. (b) Simplified T mode.

The Drain Equivalent Circuit

Figure 15(a) shows the MOSFET with Thévenin sources connected to the gate and source leads. We wish to solve for the Norton equivalent circuit seen looking into the drain. The circuit consists of a parallel current source $i_{d(sc)}$ and resistor r_{id} connecting between the drain and ground. The value of $i_{d(sc)}$ is the drain current with $v_d = 0$, i.e. with the drain node grounded. From the simplified T model circuit in Figure 15(b), this current is given by

$$i_{d(sc)} = i'_d + i_0 \simeq i'_d \tag{57}$$

where the approximation assumes that the current i_0 through r_0 is small compared to i'_d. This is usually a very good approximation because r_0 is a large value resistor. We call it the "r_0 approximation" when the current i_0 is neglected. In many cases, r_0 is taken to be an infinite resistor, in which case the approximation is exact.

To solve for i'_d, we can write the loop equation

$$\frac{v_{tg}}{1 + \chi} - v_{ts} = i'_s r'_s + i_s R_{ts} = i'_s r'_s + (i'_s + i_0) R_{ts} = i'_d r'_s + (i'_d + i_0) R_{ts} \simeq i'_d (r'_s + R_{ts}) \tag{58}$$
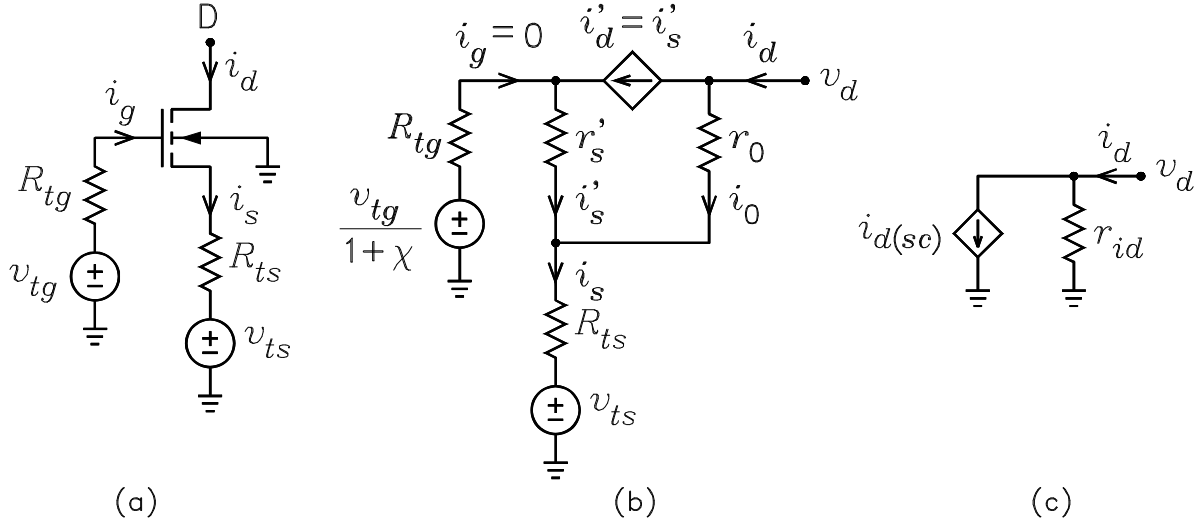
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Figure 15: (a) MOSFET with Thévenin sources connected to the gate and the source. (b) Simplified T model of the circuit. (c) Norton equivalent drain circuit.

From this equation, it follows that we can write

$$i_{d(sc)} = i'_d = G_m \left(v_{tg} - v_{ts} \right) \tag{59}$$

where G_m is an equivalent transconductance given by

$$G_m = \frac{1}{r'_s + R_{ts}} \overset{or}{=} \frac{1}{\dfrac{r_s}{1+\chi} + R_{ts}} \overset{or}{=} \frac{1}{\dfrac{1}{(1+\chi)\, g_m} + R_{ts}} \tag{60}$$

We next solve for the resistance r_{id} seen looking into the drain node. Consider the drain current i_d to be an independent current source and set $v_{tg} = v_{ts} = 0$. We can write

$$v_d = i_0 r_0 + i_s R_{ts} = \left(i_d - i'_d \right) r_0 + i_s R_{ts} = i_d \left(r_0 + R_{ts} \right) - i'_d r_0 \tag{61}$$

$$i'_d = i'_s = \frac{v_{gs}}{r'_s} = -\frac{i_s R_{ts}}{r'_s} = -\frac{i_d R_{ts}}{r'_s}$$

where $v_{gs} = -v_s = -i_s R_{ts}$ and $i_s = i_d$ have been used. Substitution of i'_d from the second equation into the first equation yields

$$v_d = i_d \left(r_0 + R_{ts} \right) - i'_d r_0 = i_d \left(r_0 + R_{ts} \right) + \frac{i_d R_{ts}}{r'_s} r_0 = i_d \left[r_0 \left(1 + \frac{R_{ts}}{r'_s} \right) + R_{ts} \right] \tag{62}$$

It follows that the drain resistance is given by

$$r_{id} = \frac{v_d}{i_d} = r_0 \left(1 + \frac{R_{ts}}{r'_s} \right) + R_{ts} \overset{or}{=} r_0 \left[1 + (1+\chi) \frac{R_{ts}}{r_s} \right] + R_{ts} \overset{or}{=} r_0 \left[1 + (1+\chi)\, g_m R_{ts} \right] + R_{ts} \tag{63}$$

Note that no approximations have been made in solving for r_{id}.

In summary, the small-signal Norton equivalent circuit seen looking into the drain of a FET is a current source $i_{d(sc)}$ in parallel with a resistor r_{id} given by

$$i_{d(sc)} = i'_d = G_m \left(\frac{v_{tg}}{1+\chi} - v_{ts} \right) \tag{64}$$

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$$G_m = \frac{1}{r'_s + R_{ts}} \overset{\text{or}}{=} \frac{1}{\dfrac{r_s}{1+\chi} + R_{ts}} \overset{\text{or}}{=} \frac{1}{\dfrac{1}{(1+\chi)\,g_m} + R_{ts}} \tag{65}$$

$$r_{id} = r_0\left(1 + \frac{R_{ts}}{r'_s}\right) + R_{ts} \overset{\text{or}}{=} r_0\left[1 + (1+\chi)\frac{R_{ts}}{r_s}\right] + R_{ts} \overset{\text{or}}{=} r_0\left[1 + (1+\chi)\,g_m R_{ts}\right] + R_{ts} \tag{66}$$

where v_{tg} and v_{ts}, respectively, are the Thévenin voltages seen looking out of the gate and source and R_{ts} is the Thévenin resistance in series with v_{ts}. Note that R_{tg} does not appear in the equations because the current through it is zero.

The Source Equivalent Circuit

The source equivalent circuit is derived above for the case where the body lead is connected to the MOSFET gate. The circuit derived here is for the case where the body is connected to signal ground. Figure 16(a) shows the MOSFET symbol with a Thévenin equivalent source connected to the gate. The equation for the source voltage v_s follows from the simplified T model circuit in Figure 14(b). It is given by

$$v_s = \frac{v_{tg}}{1+\chi} - i'_s r'_s = \frac{v_{tg}}{1+\chi} - (i_s - i_0)\,r'_s \simeq \frac{v_{tg}}{1+\chi} - i_s r'_s \tag{67}$$

where the approximation assumes that i_0 is small compared to i_s. It follows that the source equivalent circuit consists of a voltage source $v_{s(oc)}$ in series with a resistance r_{is} given by

$$v_{s(oc)} = \frac{v_{tg}}{1+\chi} \qquad r_{is} = r'_s = \frac{r_s}{1+\chi} = \frac{1}{(1+\chi)\,g_m} \tag{68}$$

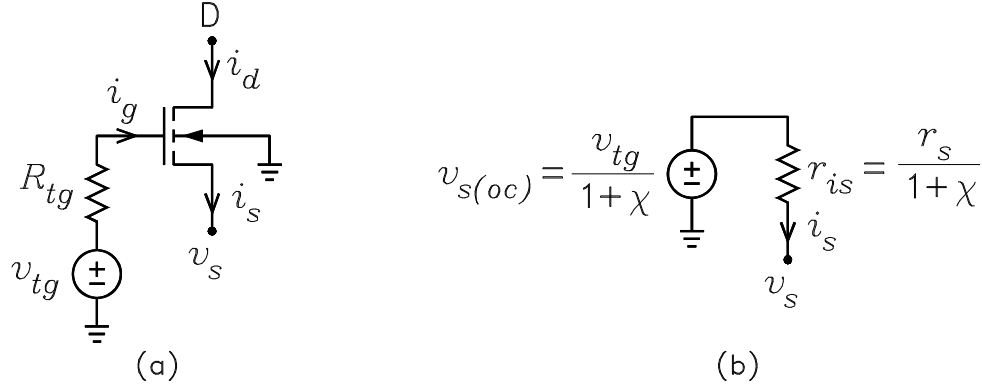The circuit is shown in Figure 16(b).

Figure 16: (a) MOSFET with Thevenin source connected to the gate and the body connected to signal ground. (b) Source equivalent circuit.

Summary of Models

$$i_{d(sc)} = i'_d = G_m\left(\frac{v_{tg}}{1+\chi} - v_{ts}\right) \tag{69}$$

$$G_m \overset{\text{or}}{=} \frac{1}{r'_s + R_{ts}} \overset{\text{or}}{=} \frac{1}{\dfrac{r_s}{1+\chi} + R_{ts}} \overset{\text{or}}{=} \frac{1}{\dfrac{1}{g_m(1+\chi)} + R_{ts}} \overset{\text{or}}{=} \frac{1}{r_{is} + R_{ts}} \tag{70}$$

$$r_s = \frac{1}{g_m} \qquad r_{is} = r'_s = \frac{r_s}{1+\chi} \overset{\text{or}}{=} \frac{1}{g_m(1+\chi)} \tag{71}$$
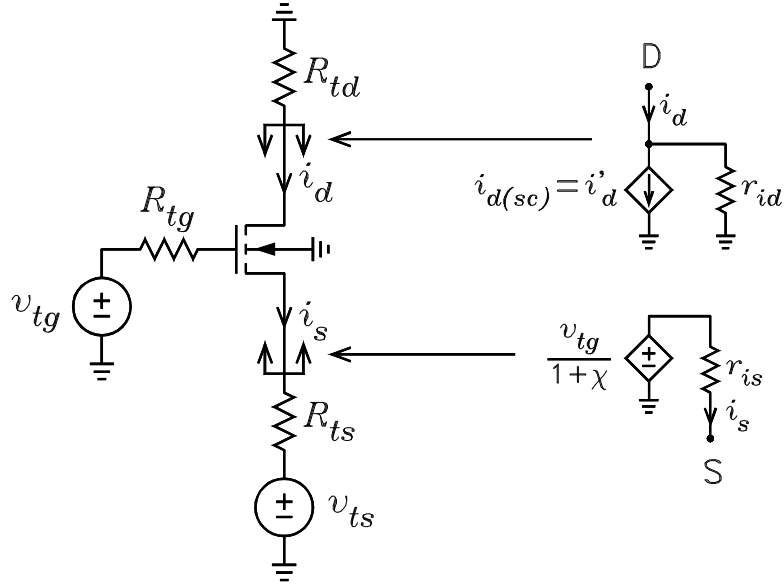
Figure 17: Summary of the equivalent circuits.

$$r_{id} = r_0 \left(1 + \frac{R_{ts}}{r_s'}\right) + R_{ts} \overset{\text{or}}{=} r_0 \left[1 + (1 + \chi)\frac{R_{ts}}{r_s}\right] + R_{ts} \overset{\text{or}}{=} r_0 \left[1 + (1 + \chi) g_m R_{ts}\right] + R_{ts} \tag{72}$$

$$r_{ig} = \infty \tag{73}$$

Set $\chi = 0$ when the body is connected to the source or when the body and the source are connected to the same node.

Small-Signal High-Frequency Models

Figures 18 and 19 show the hybrid-π and T models for the MOSFET with the gate-source capacitance c_{gs}, the source-body capacitance c_{sb}, the drain-body capacitance c_{db}, the drain-gate capacitance c_{dg}, and the gate-body capacitance c_{gb}added. These capacitors model charge storage in the device which affect its high-frequency performance. The first three capacitors are given by

$$c_{gs} = \frac{2}{3} W L C_{ox} \tag{74}$$

$$c_{sb} = \frac{c_{sb0}}{\left(1 + V_{SB}/\psi_0\right)^{1/2}} \tag{75}$$

$$c_{db} = \frac{c_{db0}}{\left(1 + V_{DB}/\psi_0\right)^{1/2}} \tag{76}$$

where V_{SB} and V_{DB} are dc bias voltages; c_{sb0} and c_{db0} are zero-bias values; and ψ_0 is the built-in potential. Capacitors c_{gd} and c_{gb} model parasitic capacitances. For IC devices, c_{gd} is typically in the range of 1 to 10 fF for small devices and c_{gb} is in the range of 0.04 to 0.15 fF per square micron of interconnect.
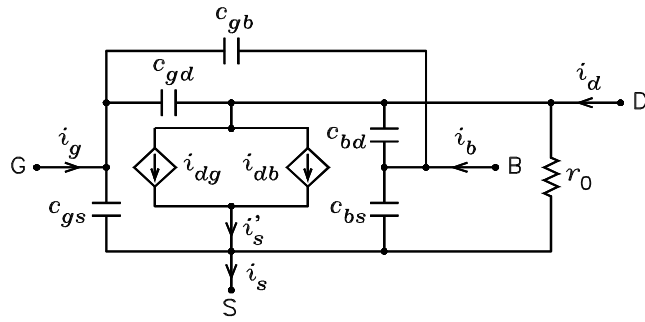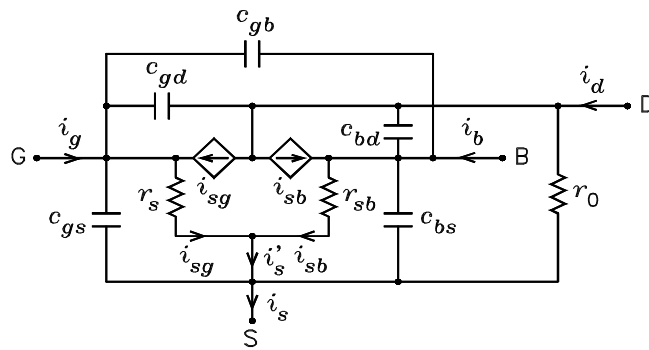
Figure 18: High-frequency hybrid-π model.

Figure 19: High-frequency T model.