Georgia Institute of Technology
School of Electrical and Computer Engineering
ECE 4435 Op Amp Design Laboratory Fall 2005

Design Project 1
An Effects Box for Electric Guitars

Object

The object of this project is to design, assemble, and evaluate an effects box for an electric guitar. The box is to generate a distortion signal that can be added in varying amounts to the signal output from the guitar pickup to modify the sound of the guitar. The distortion is to be generated in two independent circuits. The first circuit is to generate second order harmonic distortion. The second circuit is to generate clipping distortion. The outputs from these circuits are to be added independently in varying amounts to the signal output from the pickup.

Many musicians say that second-order harmonic distortion adds a richness to a guitar signal. This distortion is to be generated by a JFET differential amplifier in which the output signal is taken as a common-mode signal. Clipping of the pickup signal adds a rough raspy effect to the sound of the guitar. If it is used in moderation, it causes a note to have a slightly different tonality. If it is used heavily, it gives rise to the term "heavy metal."

Description of the Circuit

The circuit is to have an input resistance of 10 kΩ. The input stage is to have a voltage gain that can be varied from 0 to 10. The nominal signal level at the output of this stage can be considered to have an rms voltage of 1 V. The signal output from the input stage is to be applied to both the second harmonic generator and the clipper. These circuits are to be followed by a summing amplifier which allows the outputs from the effects circuits to be summed in varying amounts and fed to the output stage. With a 1 V rms level from the input stage, the gain of the output stage is to be variable such that the rms output level can be adjusted to be in the range of 0 to 4 V. The output signal is to be ac coupled with an output resistance of 100 Ω.

Second Harmonic Generator: The second harmonic generator is to consist of a JFET differential amplifier. The common-mode output current of the diff amp is to be converted into a voltage that drives one input to the summing amplifier. The basic circuit of the JFET diff amp is shown in Figure 1. The signal which drives the diff amp must be a differential signal that is derived from an unbalanced signal to balanced signal converter. The resistors labeled R_S and the potentiometer labeled R_P set the source bias current in each JFET. The JFETs should be biased at approximately $I_{DSS}/2$, where I_{DSS} is the drain current with $V_{GS} = 0$. It is preferable to match the two JFETs. Because it is impossible to obtain an exact match, the potentiometer can be used to offset the dc bias currents in the two JFETs to optimize the operation of the circuit. The capacitor C is to be large enough so that it is essentially a short circuit for frequencies above 20 Hz. This will be approximately true if $C > 2.5/r_s\pi f$, where $r_s = 1/g_m$ and g_m is the transconductance of each JFET at the dc bias point.

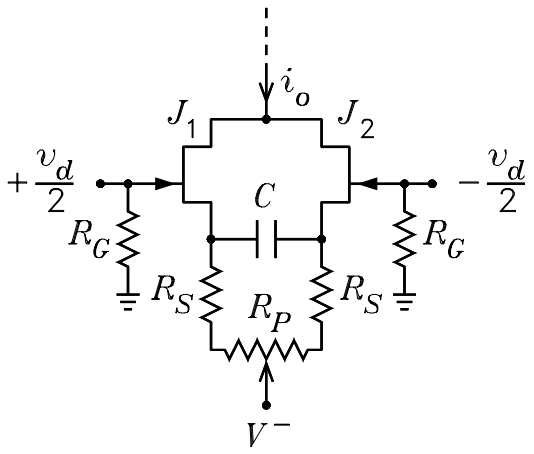

Figure 1: Second harmonic generator circuit.

The JFET that is available in the laboratory is the 2N5457 n-channel JFET. Its drain current can be written in two ways

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_{TO}}\right)^2 = \beta\,(v_{GS} - V_{TO})^2$$

where $\beta = I_{DSS}/V_{TO}^2$ and V_{TO} is negative. Typical range values for I_{DSS} and V_{TO} are $2\,\text{mA} \le I_{DSS} \le 3\,\text{mA}$ and $-3\,\text{V} \le V_{TO} \le -2\,\text{V}$. The transconductance is given by

$$g_m = \frac{-2}{V_{TO}}\sqrt{I_D I_{DSS}} = 2\sqrt{\beta I_D}$$

If the 2N5457 is biased at $I_{DSS}/2$, its transconductance has the value $g_m = -\sqrt{2}I_{DSS}/V_{TO}$. The worst case value for r_s in calculating the value of C is the smallest value. This translates into the largest value of g_m. This occurs with $I_{DSS} = 3\,\text{mA}$ and $V_{TO} = -2\,\text{V}$ to obtain $r_s = \sqrt{2}/0.003 = 471.4\,\Omega$. For $f = 20\,\text{Hz}$, it follows that the value of the capacitor C in the circuit above should satisfy

$$C > \frac{2.5}{471.4 \times \pi \times 20} = 84\,\mu\text{F}$$

The capacitor should be a non-polar unit. In this case it is realized as the series connection of two capacitors of value $168\,\mu\text{F}$. The nearest larger value capacitor in the lab is a $220\,\mu\text{F}$ capacitor.

Let $R'_S = R_S + R_P/2$. If V_{GS} is small compared to V^-, the drain current in each JFET is given by

$$I_D = \frac{-V^-}{R'_S}$$

This equation can be used to calculate a first cut value for R'_S. A more exact equation for I_D is

$$I_D = \left(\frac{-b + \sqrt{b^2 - 4ac}}{2a}\right)^2$$

where

$$a = R'_S \qquad b = \frac{1}{\sqrt{\beta}} \qquad c = V^- + V_{TO}$$

Let the differential input voltage to the diff amp be given by $v_d = V_p \cos(\omega t)$. You should show that the ac component of the output current is given by

$$i_o = \frac{I_{DSS} V_p^2}{4 V_{TO}^2} \cos(2\omega t)$$

which is at the second harmonic frequency. This current must be converted into a voltage which becomes the second harmonic distortion term. This signal is to be ac coupled from the output of the second-harmonic generator.

Clipping Generator: The clipping of the guitar signal can be easily generated with a diode clipping circuit. The diodes can be connected in parallel with the feedback resistor of an inverting amplifier or as the shunt element of a voltage divider. A means of varying the amount of clipping on the waveform by varying a potentiometer is to be part of the circuit. A desirable feature would be to adjust the "hardness" of clipping by varying a potentiometer. You are free to implement the clipping in any way that you choose. The basic objective is to be able to vary the amount of clipping on the signal.

Suggested Design Methodology: You should begin by drawing a block diagram of the circuit. After that, the individual circuits for each block can be designed, assembled, and tested. After each individual circuit is operational, the circuits can be connected together to complete the design.