Design Project—Fall 2007

Objective

The objective of this experiment is to design, simulate, evaluate experimentally, and document a low-noise discrete BJT amplifier. The equivalent input noise of the amplifier is to be minimized.

Specifications

The topology used for the amplifier consists of a singled ended input and output and either a unipolar or bipolar dc power supplies.

The specifications for the amplifier are:

- DC Power Supplies: either $\pm 15\,\text{V}$, or $+15$ V, or $-15\,\text{V}$.
- Midband Small Signal Voltage Gain: 30 dB
- Maximum Input Signal 200 mV rms
- Lower Half-Power Frequency: 20 Hz or less.
- Upper Half-Power Frequency: 20 kHz or greater
- THD (total harmonic distortion): less than 0.4% corresponding to an output signal level of +10 dBm for an input sine wave with a frequency of 2 kHz
- Source Resistance: $600\,\Omega$
- Load Resistance: $600\,\Omega$
- Input noise voltage over the band 20 Hz to 20 kHz to be minimized

Simulation

The initial design should be verified with a SPICE simulation. This simulation must precede the circuit assembly.

The default values for `IS`, `BF`, `RB`, `VA`, `CJC`, `CJE`, and `TF` for the BJT transistors are not to be used for the simulation. Instead, use the values obtained from curve tracer measurements or manufacturers' data sheets. The value of the base spreading resistance measured in a previous experiment is to be used as `RB`.

A noise simulation of the circuit should be made which predicts the signal-to-noise ratio corresponding to an output signal level of +10 dBm into $600\,\Omega$ and the noise figure of the amplifier. Use SPICE to evaluate the noise performance at values of bias currents other than the optiumum to demonstrate that the optimum does indeed produce the best noise performance.

The SPICE analyses should include `.OP` (to verify the biasing), `.AC` (to verify the frequency response specifications and phase margin specifications), `.TRAN` (to examine the clipping and slew rate performance), `.FOUR` (to verify the distortion specification), and `.NOISE` (to verify the noise specifications).

Experimental Measurements

Assemble the designed circuit on a solderless breadboard with a $600\,\Omega$ load resistor. Use a power supply decoupling network.

Use the laboratory equipment to measure and record the amplifier:

- mid-band voltage gain
- -3 dB bandwidth
- positive and negative slew rates

- distortion @ $f = 2\,\text{kHz}$
- quiescent operating point
- output dc offset with input grounded
- equivalent input noise voltage
- signal-to-noise ratio with an input signal of 200 mV rms
- noise figure (spot noise figure @ $f = 2\,\text{kHz}$ and the total noise figure)
- bias the circuit for non optimum currents to examine whether or not the optimum bias results in the desired noise performance.

The noise measurements are made with the source grounded. The other measurements are made with the function generator as the source.

Laboratory Report

The laboratory report should simply, succinctly, and lucidly summarize the design philosophy, present the appropriate calculations, and compare the theoretical, simulation, and experimental results.

The design project will weighted as three lab reports and will graded somewhat more critically than the previous reports. Although the design project grade will in part depend on the write-up, the major criterion will be whether or not the circuit meets the design criteria.

Due Date

Friday, December 7, 2007 A. D., 6 pm EST.