An Amplifier Input Stage Design Criterion for the Suppression of Dynamic Distortions*

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A design criterion for the input stage of an amplifier is presented which can be used to eliminate the principal source of dynamic distortion mechanisms such as TIM and SID in feedback amplifiers. The criterion is developed independently of the slew rate of the amplifier or the bandwidth of the input stage and the stages which follow this stage.

0 INTRODUCTION

In feedback amplifiers, dynamic distortions such as transient intermodulation distortion (TIM) and slewing-induced distortion (SID) arise principally from the overload of the internal stage which immediately precedes that stage that sets the frequency of the dominant pole in the open-loop transfer function of the amplifier. In contemporary amplifier and operational amplifier designs, this stage is normally the input stage [1]–[5] which is most often a differential amplifier. If the input stage becomes excessively nonlinear before it clips, the amplifier is said to produce soft TIM and SID.

It is well known that the addition of local negative feedback in the form of transconductance reduction to the input stage of an amplifier can be used to reduce soft TIM and SID. This form of feedback is realized by the addition of emitter degeneration resistors for a bipolar junction transistor input stage or source degeneration resistors for a field effect transistor stage. When the technique is skillfully applied, the dominant pole lag compensation capacitor can be simultaneously reduced to realize an increase in the slew rate of the amplifier [5]. This reduces its susceptibility to hard TIM and SID.

The use of transconductance reduction in the input stage of an amplifier can also be used to prevent internal clipping of this stage. This makes it theoretically possible to design a nonslewing amplifier without the use of bandwidth reduction in the form of a low-pass filter preceding the amplifier. The technique consists of choosing the value of the transconductance reduction resistors so that the amplifier output stage will always clip before the input stage clips under worst-case signal conditions at the amplifier input and output terminals. These worst-case signal conditions are defined in the following, and a technique for calculating the minimum required value of the transconductance reduction resistors is presented.

1 INPUT STAGE DESIGN

The basic circuit model of a feedback amplifier given in Fig. 1 will be used for the analysis. The feedback ratio for this circuit is given by

$$\beta = \frac{R_2}{R_1 + R_2} \quad . \tag{1}$$

It will be assumed in the following analysis that the open-loop gain is sufficiently high so that the closed-loop gain can be written as the reciprocal of β. The input transistors are shown as bipolar junction transistors. The analysis is also valid for field-effect transistors.

Under quiescent conditions, the current through the two emitter resistors labeled R_E in Fig. 1 is $I_0/2$. When the input signal v_i goes positive, the current I_{E1} increases and the current I_{E2} decreases, and conversely if v_i goes negative. If neither current decreases to zero under worst-case signal conditions, then the input stage cannot clip and the amplifier cannot slew. In the following, a condition that I_{E2} not reduce to zero when v_i goes

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positive will be derived. Because of symmetry, the condition that I_{E1} not reduce to zero when v_i goes negative is the same.

Under dynamic signal conditions, the current I_{E2} can be written

$$I_{E2} = \frac{I_0}{2} - \frac{(v_i - v_{BE1}) - (v_f - v_{BE2})}{2R_E}$$

$$= \frac{I_0}{2} - \frac{v_i - v_f}{2R_E} + \frac{v_{BE1} - v_{BE2}}{2R_E} . \quad (2)$$

For v_i increasing, $v_{BE1} \geq v_{BE2}$, and the inequality

$$I_{E2} \geq \frac{I_0}{2} - \frac{v_i - v_f}{2R_E} \quad (3)$$

holds. It follows from this that if

$$\frac{I_0}{2} - \frac{v_i - v_f}{2R_E} \geq 0 \quad (4)$$

then I_{E2} can never be zero for v_i increasing. This relation can be rewritten in the form

$$R_E \geq \frac{v_i - v_f}{I_0} . \quad (5)$$

In order to use Eq. (5) to determine the minimum value of R_E given the current I_0, it is necessary to specify the worst-case maximum value of $v_i - v_f$. It will be assumed that v_i is constrained to be less than or equal to the value that causes the amplifier output stage to clip. Let this output clipping level be $v_{o\,max}$. For a closed-loop gain equal to the reciprocal of the feedback ratio β, it thus follows that $v_i - v_f$ is maximized when

$$v_i = \beta v_{o\,max} \quad (6)$$

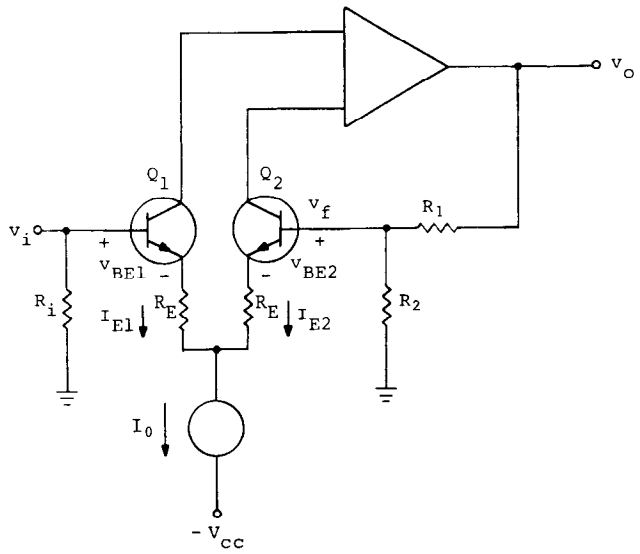

Fig. 1. Basic circuit model used for the analysis which explicitly shows the typical input stage and resistive feedback network of a contemporary audio amplifier. v_i—input voltage; v_o—output voltage; v_f—feedback voltage; v_{BE1}, v_{BE2}—base-to-emitter voltages of transistors Q_1 and Q_2, respectively; I_{E1}, I_{E2}—emitter currents of Q_1 and Q_2, respectively.

and

$$v_f = -\beta v_{o\,max} . \quad (7)$$

Thus for worst-case conditions R_E must satisfy the inequality

$$R_E \geq \frac{2\beta v_{o\,max}}{I_0} \quad (8)$$

If Eq. (8) holds, the input stage cannot clip if the amplifier output voltage is initially at one clipping level and the input signal instantaneously changes so as to cause the output voltage to swing to the opposite clipping level. An amplifier so designed cannot slew from overload of its input stage and is thus theoretically free of hard TIM and SID produced by this stage. Because the value of R_E predicted by Eq. (8) is relatively large compared to values normally used for local negative feedback, the resulting linearity of the input stage should be such that it cannot produce soft TIM and SID.

As an example, consider a 100-W amplifier operating with a closed-loop gain of 20 and having a bias current in the input differential amplifier of 2 mA. The peak output signal swing is 40 V. It thus follows from Eq. (8) that R_E must be 2000 Ω or larger to prevent clipping of the input stage under worst-case signal conditions.

It is interesting to note that in an amplifier with no overall feedback, $v_f = 0$ in Eq. (7) and the minimum required value for R_E is one-half the value predicted by Eq. (8). In this case the feedback ratio β in Eq. (8) must be interpreted as the reciprocal of the amplifier gain. Conversely, it may be concluded that the use of feedback reduces the input stage overload margin by a factor of 2, provided the amplifier gain from input to output is held constant.

2 CONCLUSIONS

A simple design criterion for the input stage of an amplifier which permits realization of a slew-free design has been described. The procedure allows the designer to calculate the minimum value of the input stage transconductance reduction resistors which will prevent clipping of the input stage under worst case input and output signal conditions. The technique is applicable to a differential amplifier input stage that uses either bipolar junction or field effect transistors. Because the criterion is based on static parameters only, it is postulated that the terms "transient" and "dynamic" are incorrect terms when applied to distortion caused by overload of the input stage of an amplifier.

3 REFERENCES

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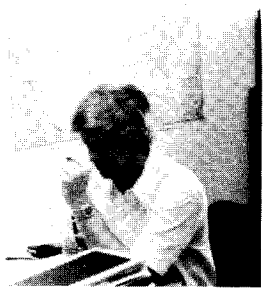

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