Noise Relations for Parallel Connected Transistors*

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The mean-square equivalent noise input voltage is calculated for an amplifier input stage for the case where the stage consists of a number of identical devices connected in parallel. The devices that are considered are the BJT and the MOSFET. The effect on noise of the number of devices and the bias current in each device is investigated.

0 INTRODUCTION

A technique of low-noise amplifier design is to realize the input stage with a number of identical active devices connected in parallel [1]–[7]. If the signal outputs of the devices are correlated and the noise outputs are not correlated, the signal-to-noise ratio (SNR) is improved by 3 dB each time the number of devices is doubled. However, this is true only if the thermal noise generated by the resistance of the signal source at the input is negligible. If not, there is a correlated noise component at the output of each device due to the source noise. This component causes the improvement in SNR for the source and amplifier in combination to be less than the 3-dB upper bound when the number of devices is doubled. In this case there is an optimum number of devices that maximizes the SNR which is dependent on the source resistance. Any number greater than this optimum causes a decrease.

This engineering report investigates the noise performance of amplifier input stages consisting of parallel bipolar junction transistors (BJTs) and parallel metal oxide semiconductor field effect transistors (MOSFETs). The noise is considered to be a minimum when the SNR is a maximum. It is shown that the parallel connection of BJTs biased at a fixed total current only results in a reduction in the thermal noise generated by the base spreading resistance. The optimum number of parallel BJTs is obtained which maximizes the SNR when the current per device is held constant. In addition, the optimum bias current per BJT is obtained which maximizes the SNR for a fixed number of devices. It is shown that the parallel connection of N identical MOSFETs biased at a fixed total current has the same noise performance as a single MOSFET having an effective channel width that is N times larger.

The notation used in the analysis is as follows. A dc bias value is denoted by an uppercase letter with an uppercase subscript, such as I_C; a small-signal value is denoted by a lowercase letter with a lowercase subscript, such as v_n; and a mean-square value is denoted by a bar over the square of the variable, such as $\overline{v_n^2}$. The mean-square value of a variable is the square of its rms value. Circuit symbols for independent signal sources are round. Symbols for dependent sources are diamond shaped. Symbols for noise sources are square.

1 PARALLEL CONNECTED BJTs

Fig. 1 shows the signal circuit of the input stage of an amplifier consisting of N identical BJTs connected in parallel. Each is represented by its v_n–i_n noise model, where v_{nj} and i_{nj} represent, respectively, the input noise voltage and current for the jth device. There are two signal sources, v_{sb} and v_{se}. Each is modeled as a Thévenin source, where v_{tsb} and v_{tse} are the thermal noise voltages generated by the source resistances R_{SB} and R_{SE}, respectively. The circuit is a common-emitter (CE) amplifier if $v_{se} = 0$ and a common-base (CB) amplifier if $v_{sb} = 0$. By analyzing the circuit with the two sources, the noise for both configurations can be calculated without repeating the analysis. It is shown that the equivalent noise input voltage can be considered to be in series with either input source.

The base spreading resistance r_x of each BJT in Fig. 1 is shown as an external resistor. This resistor is considered to be noiseless in the model, for its noise is con-

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tained in v_n. The noise voltage and the noise current in the BJT noise model are given by [7]

$$v_n = v_{tx} + i_{shc}\frac{V_T}{I_C} \tag{1}$$

$$i_n = i_{shb} + i_{fb} + \frac{i_{shc}}{\beta}. \tag{2}$$

In these equations, v_{tx} is the thermal noise generated by r_x, i_{shc} is the shot noise in the collector bias current I_C, i_{shb} is the shot noise in the base bias current I_B, i_{fb} is the flicker noise in the base bias current, $\beta = I_C/I_B$ is the current gain, and $V_T = kT/q$ is the thermal voltage, with k Boltzmann's constant, T the absolute temperature, and q the electronic charge.

The noise sources have the following mean-square values [6]–[8]:

$$\overline{v_{tsb}^2} = 4kTR_{SB}\Delta f \tag{3}$$

$$\overline{v_{tse}^2} = 4kTR_{SE}\Delta f \tag{4}$$

$$\overline{v_{tx}^2} = 4kTr_x\Delta f \tag{5}$$

$$\overline{i_{shc}^2} = 2qI_C\Delta f \tag{6}$$

$$\overline{i_{shb}^2} = 2qI_B\Delta f \tag{7}$$

$$\overline{i_{fb}^2} = K_f I_B\frac{\Delta f}{f} \tag{8}$$

where Δf is the frequency band in hertz over which the noise is measured, K_f is the flicker noise coefficient, and f is the frequency in hertz. It is commonly assumed that the sources are independent, that is, not correlated.

The analysis is simplified if all transistor noise sources are represented as voltage sources in series with R_{SB} and R_{SE}. To put the circuit into this form, the first step is to move the upper lead of each i_n source from the right node of its corresponding r_x to the left node of r_x. This requires changing the value of the v_{nj} sources to v'_{nj}, given by

$$v'_{nj} = v_{nj} + i_{nj}r_x. \tag{9}$$

Next replace each i_n source with two series sources, each having the value i_n, with the common node between the two grounded. All currents in the transistors are independent of these source transformations.

The next step is to replace the circuits seen looking out of the parallel connected bases and emitters with Thévenin equivalent circuits and to reverse the order of each v'_n and r_x in series with the bases. The resulting circuit is shown in Fig. 2, where v_{nb} and v_{ne} are given by

$$v_{nb} = R_{SB}\sum_{j=1}^{N} i_{nj} \tag{10}$$

$$v_{ne} = R_{SE}\sum_{j=1}^{N} i_{nj}. \tag{11}$$

The last step is to replace the v'_{nj} sources with a single source equal to the common-mode value of the N sources at the position $\times$ in Fig. 2. The circuit is shown in Fig. 3, where v'_n is given by

$$v'_n = \frac{1}{N}\sum_{j=1}^{N} v'_{nj} = \frac{1}{N}\sum_{j=1}^{N}(v_{nj} + i_{nj}r_x). \tag{12}$$

Because the latter step is not obvious, a simple proof is presented for the case $N = 3$. It is straightforward to

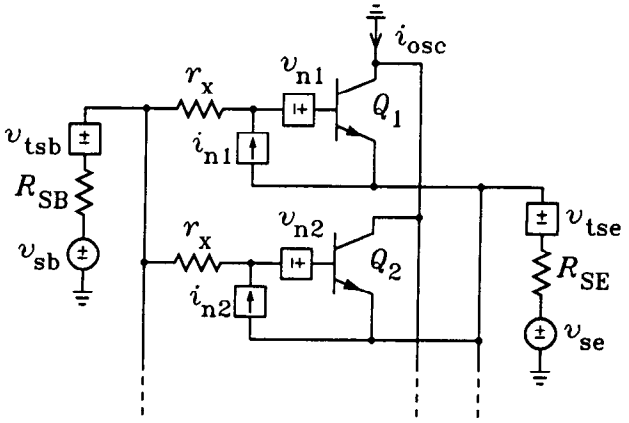

Fig. 1. Signal circuit for parallel connected BJT stage.

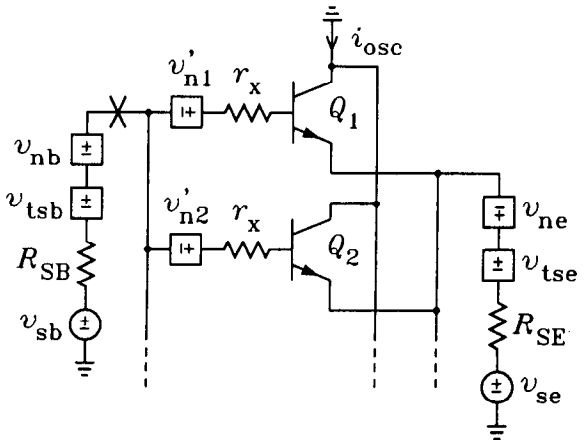

Fig. 2. BJT circuit with i_{nj} sources removed.

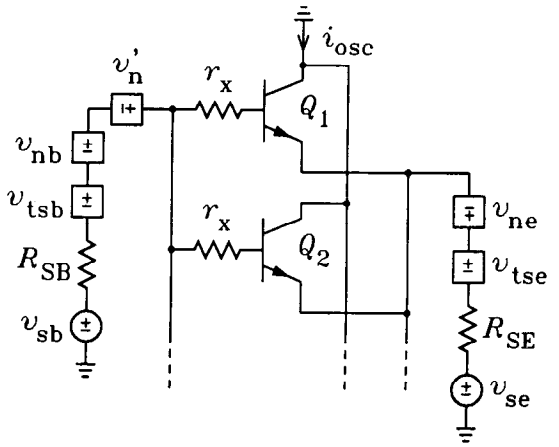

Fig. 3. BJT circuit with v'_{nj} sources removed.

extend the proof for other values of N. For simplicity, let the three noise voltage sources be represented by x, y, and z. We can write $x = a + b + c$, $y = a - b + d$, and $z = a - c - d$, where $a = (x + y + z)/3$, $b = (x - y)/3$, $c = (x - z)/3$, and $d = (y - z)/3$. Because of linearity, superposition of a, b, c, and d can be used to obtain the total response of the circuit. When a alone is active, the three sources are equal and the response of the circuit is the same as for a single source a at the position $\times$ in Fig. 2. When b alone is active, Q_1 and Q_2 are driven differentially and the collector output currents cancel. The same happens between Q_1 and Q_3 when c is active and between Q_2 and Q_3 when d is active. This completes the proof.

The T model of the BJT is shown in Fig. 4, where $r_e = V_T/I_E$ is the intrinsic emitter resistance, I_E is the emitter bias current, and $\alpha = I_C/I_E$. When the model is substituted for the transistors in the circuit of Fig. 3, it follows by symmetry that all transistors have the same currents and the same voltages at the B' nodes. Therefore, the T models can be combined in parallel to form the final circuit of Fig. 5. The following loop equation cn be written:

$$v_{sb} - v_{se} + v_{tsb} - v_{tse} + v_{nb} + v_{ne} + v_n' = Ni_b\left(R_{SB} + \frac{r_x}{N}\right) + Ni_e\left(\frac{r_e}{N} + R_{SE}\right). \tag{13}$$

Because $i_b = (1 - \alpha)\, i_e$, it follows that i_e can be solved for to obtain

$$i_e = \frac{v_{sb} - v_{se} + v_{tsb} - v_{tse} + v_{nb} + v_{ne} + v_n'}{N(1 - \alpha)(R_{SB} + r_x/N) + N(r_e/N + R_{SE})}. \tag{14}$$

The short-circuit output current is given by $i_{osc} = N\alpha i_e$. It follows that the equivalent noise voltage v_{ni} in series with either v_{sb} or v_{se}, which generates the same noise current in i_{osc} as all noise sources in the circuit, is given by

$$\begin{aligned} v_{ni} &= v_{tsb} - v_{tse} + v_{nb} + v_{ne} + v_n' \\ &= v_{tsb} - v_{tse} + \left(R_{SB} + \frac{r_x}{N} + R_{SE}\right)\sum_{j=1}^{N} i_{nj} + \frac{1}{N}\sum_{j=1}^{N} v_{nj}. \end{aligned} \tag{15}$$

This is the equivalent noise input voltage for both the CE and the CB configurations.

With the aid of Eqs. (1) and (2), the equation for v_{ni} can be reduced to

$$v_{ni} = v_{tsb} - v_{tse} + \frac{1}{N}\sum_{j=1}^{N} v_{txj} + \left(R_{SB} + \frac{r_x}{N} + R_{SE}\right)\sum_{j=1}^{N}(i_{shbj} + i_{fbj}) + \left(\frac{R_{SB} + r_x/N + R_{SE}}{\beta} + \frac{V_T}{NI_C}\right)\sum_{j=1}^{N} i_{shcj}. \tag{16}$$

This can be converted to a mean-square voltage to obtain

$$\overline{v_{ni}^2} = 4kT\left(R_{SB} + \frac{r_x}{N} + R_{SE}\right)\Delta f + \left(R_{SB} + \frac{r_x}{N} + R_{SE}\right)^2\left(2qNI_B\Delta f + \frac{K_f NI_B^2\Delta f}{f}\right) + \left(\frac{R_{SB} + r_x/N + R_{SE}}{\beta} + \frac{V_T}{NI_C}\right)^2 2qNI_C\Delta f. \tag{17}$$

The first term in this equation arises from the thermal noise generated by R_{SB}, r_x, and R_{SE}. The second term arises from the shot noise and flicker noise in I_B. The third term arises from the shot noise in I_C.

The SNR of the stage is given by

$$\text{SNR} = \frac{\overline{v_s^2}}{\overline{v_{ni}^2}} \tag{18}$$

where $\overline{v_s^2} = \overline{v_{sb}^2}$ for the CE configuration and $\overline{v_s^2} = \overline{v_{se}^2}$ for the CB configuration. It follows that the SNR is maximized when $\overline{v_{ni}^2}$ is minimized. It can be concluded from Eq. (17) that a first step in minimizing the noise is to make R_{SE} as small as possible for the CE configuration and R_{SB} as small as possible for the CB configuration. For each configuration it is assumed that the source resistance is fixed and cannot be varied. For example, the source resistance might be the output resistance of a low-level transducer such as a microphone or a tape head.

Eq. (17) is valid only at frequencies where the effects of the BJT base–emitter diffusion capacitance c_π and the collector–base depletion capacitance c_μ can be neglected. With devices in parallel, these capacitors combine in parallel in the equivalent circuit. This can result in a degradation in the high-frequency performance or in the stability of the circuit. Because c_π is proportional to I_C, the parallel combination of these capacitors does not change with N if the total stage current is held constant.

1.1 Noise Factor

The noise factor of an amplifier is given by

$$F = \frac{\overline{v_{ni}^2}}{\overline{v_{ts}^2}} = 1 + \frac{\overline{v_n^2} + 2\rho\sqrt{\overline{v_n^2}}\sqrt{\overline{i_n^2}}R_S + \overline{i_n^2}R_S^2}{4kTR_S\Delta f} \tag{19}$$

where $v_{ni} = v_{ts} + v_n + i_nR_S$ is the equivalent noise input voltage, v_{ts} is the thermal noise generated by the source resistance R_S, v_n is the input noise voltage, i_n is the input noise current, and ρ is the correlation coeffi-

cient between v_n and i_n.

The value of R_S which minimizes F is called the optimum source resistance R_{SO}. It is obtained by setting $dF/dR_S = 0$ and solving for R_S, and is given by

$$R_{SO} = \sqrt{\frac{\overline{v_n^2}}{\overline{i_n^2}}}. \tag{20}$$

The corresponding value of F is called the optimum noise factor and is given by

$$F_{opt} = 1 + \frac{\overline{v_n^2}(1 + \rho)}{2kTR_{SO}\Delta f}. \tag{21}$$

To solve for R_{SO} for the parallel BJT stage, a CE configuration is assumed so that R_{SB} is the source resistance and v_{tsb} is the thermal noise generated by the source. In this case, the equivalent noise input voltage v_{ni} is written

$$v_{ni} = v_{tsb} + v_n + i_n R_{SB}. \tag{22}$$

When this is compared to Eq. (15), it follows that the input noise voltage and current are given by

$$v_n = -v_{tse} + \left(\frac{r_x}{N} + R_{SE}\right)\sum_{j=1}^{N} i_{nj} + \frac{1}{N}\sum_{j=1}^{N} v_{nj} \tag{23}$$

$$i_n = \sum_{j=1}^{N} i_{nj}. \tag{24}$$

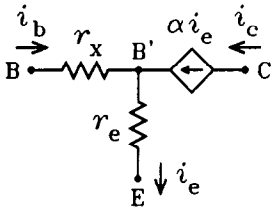

Fig. 4. T model of BJT.

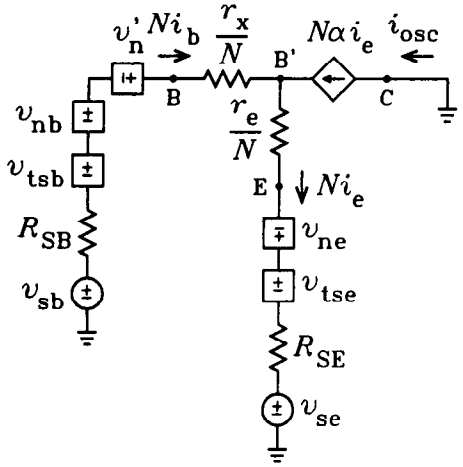

Fig. 5. Final BJT circuit.

These can be converted into mean-square values and substituted into Eq. (20) to obtain

$$R_{SO} = \left[\left(\frac{r_x}{N} + R_{SE}\right)^2 + \frac{2\beta V_T(r_x + R_{SE} + V_T/2I_C)}{N^2 I_C(1 + 1/\beta)}\right]^{1/2} \tag{25}$$

where it is assumed that the frequency is high enough so that flicker noise can be neglected. If $R_S \neq R_{SO}$, resistors should never be added in series or in parallel with the source to make the effective source resistance equal to R_{SO}. Although this minimizes F, the SNR is decreased. This is called the noise factor fallacy.

1.2 Constant Stage Current

If the total bias current in the parallel stage is held constant, the bias current per device is proportional to $1/N$. It follows that NI_C and NI_B are constant in Eq. (17). In this case, the total noise caused by base current shot and flicker noise and collector current shot noise is constant. The only reduction in $\overline{v_{ni}^2}$ that can be achieved by increasing N is in the thermal noise generated by r_x. If $R_{SB} + R_{SE} >> r_x/N$, an increase in N results in little or no improvement in the noise.

If N is made too large, the decrease in I_C can affect the performance of the BJT if I_C becomes too small. If the devices become starved for collector current, the current gain β may drop. This can cause the noise performance to deteriorate.

1.3 Constant Device Current

If $R_{SB} = R_{SE} = 0$ and I_C is held constant, the total bias current for the stage is proportional to N. It follows from Eq. (17) that $\overline{v_{ni}^2} \propto 1/N$. Thus the noise is reduced by 3 dB each time N is doubled. For $R_{SB} > 0$ or $R_{SE} > 0$, the noise is reduced by less than 3 dB when N is doubled.

The power dissipated in the stage is proportional to the square of the total bias current. It follows that the power increases as N^2 for constant device current. Thus a limitation on the maximum acceptable power dissipation translates into a limit on N.

1.4 Optimum *N*

If I_C is fixed, there is a value of N that minimizes the noise. When N is increased above this value, the noise increases. The optimum value of N that minimizes $\overline{v_{ni}^2}$ can be obtained by setting $d\overline{v_{ni}^2}/dN = 0$ and solving for N. It is given by

$$N_{opt} = \frac{\beta V_T}{I_C(R_{SB} + R_{SE})}\sqrt{\left(1 + \frac{I_C r_x}{\beta V_T}\right)^2 - \frac{\beta}{1 + \beta}} \tag{26}$$

where it is assumed that the frequency is high enough so that the flicker noise can be neglected. For this value of N it is straightforward to show that the minimized mean-square noise voltage is given by

$$\overline{v_{ni(min)}^2} = 4kT(R_{SB} + R_{SE})\Delta f\left(1 + \frac{1}{\beta}\right)\left(1 + \frac{I_C}{\beta V_T}[r_x + N_{opt}(R_{SB} + R_{SE})]\right). \tag{27}$$

For $N \neq N_{opt}$, it can be shown that the expression for $\overline{v_{ni}^2}$ can be written

$$\overline{v_{ni}^2} = \overline{v_{ni(min)}^2}\left[1 + \frac{0.5(N/N_{opt} + N_{opt}/N) - 1}{1 + \sqrt{1 + \beta}}\right]. \tag{28}$$

This equation shows that $\overline{v_{ni}^2}$ is the same for $N = rN_{opt}$ as it is for $N = N_{opt}/r$, where r is any positive constant.

1.5 Optimum Bias Current

If N is held constant and I_C is varied, the value of I_C that minimizes $\overline{v_{ni}^2}$ can be obtained by setting $d\overline{v_{ni}^2}/dI_C = 0$ and solving for I_C. It is given by

$$I_{C(opt)} = \frac{\beta V_T}{[N(R_{SB} + R_{SE}) + r_x]\sqrt{1 + \beta}} \tag{29}$$

where it is assumed that the frequency is high enough so that the flicker noise can be neglected. In this case, the minimized mean-square voltage is given by

$$\overline{v_{ni(min)}^2} = 4kT\left(R_{SB} + R_{SE} + \frac{r_x}{N}\right)\Delta f\frac{\sqrt{1 + \beta}}{\sqrt{1 + \beta} - 1}. \tag{30}$$

For $I_C \neq I_{C(opt)}$, the expression for $\overline{v_{ni}^2}$ can be put into the form

$$\overline{v_{ni}^2} = \overline{v_{ni(min)}^2}\left(1 + \frac{0.5[I_C/I_{C(opt)} + I_{C(opt)}/I_C] - 1}{1 + \sqrt{1 + \beta}}\right). \tag{31}$$

This equation shows that $\overline{v_{ni}^2}$ is the same for $I_C = rI_{C(opt)}$ as it is for $I_C = I_{C(opt)}/r$, where r is any positive constant.

2 PARALLEL CONNECTED MOSFETs

Fig. 6 shows the signal circuit of the input stage of an amplifier consisting of N identical MOSFETs connected in parallel. It is assumed that the body or bulk terminal of each device is connected to the source terminal. Each MOSFET is represented by its v_n noise model, where v_{nj} represents the input noise voltage for the jth device. Because the gate bias current is so minuscule in the MOSFET, there is no i_n noise source. There are two signal sources, v_{sg} and v_{ss}. For $v_{ss} = 0$, the configuration is a common-source (CS) amplifier. For $v_{sg} = 0$, it is a common-gate (CG) amplifier. The noise sources v_{tsg} and v_{tss} represent the thermal noise generated by the source resistances R_{SG} and R_{SS}, respectively.

It is assumed that the MOSFETs are biased in the saturation region. In this region the device bias voltages must satisfy $V_{DS} > V_{GS} - V_{TO}$, where V_{DS} is the drain-to-source voltage, V_{GS} is the gate-to-source voltage, and V_{TO} is the device threshold voltage.

The input noise voltage in the MOSFET model is given by [6]–[9]

$$v_n = \frac{i_{td} + i_{fd}}{g_m} \tag{32}$$

where i_{td} is the thermal noise generated in the channel, i_{fd} is the flicker noise generated in the channel, and g_m is the transconductance. The latter is given by $g_m = 2\sqrt{KI_D}$, where K is the transconductance parameter and I_D the drain bias current. The transconductance parameter is given by $K = \mu_0 C_{ox} W/2L$, where μ_0 is the average carrier mobility in the channel, C_{ox} is the gate oxide capacitance per unit area, W is the effective channel width, and L is the effective channel length.

With appropriate subscript changes, the mean-square values of v_{tsg} and v_{tss} are given by Eqs. (3) and (4). The mean-square values of the two noise currents in Eq. (32) are given by [6]–[9]

$$\overline{i_{td}^2} = 4kT\left(\frac{2g_m}{3}\right)\Delta f = \frac{16}{3}kT\sqrt{KI_D}\,\Delta f \tag{33}$$

$$\overline{i_{fd}^2} = \frac{K_f I_D \Delta f}{fL^2 C_{ox}} \tag{34}$$

where K_f is the flicker noise coefficient. It is commonly assumed that the noise sources are independent.

The MOSFET circuit can be transformed into a circuit similar to that in Fig. 5. The transformation is similar to that for the BJT, with the exception that there are no i_n sources. The final circuit is given in Fig. 7, where the

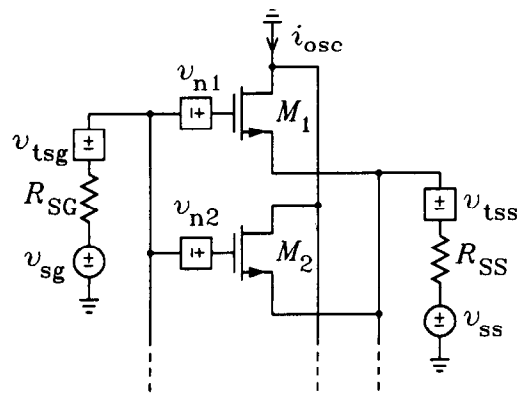

Fig. 6. Signal circuit for parallel connected MOSFET stage.

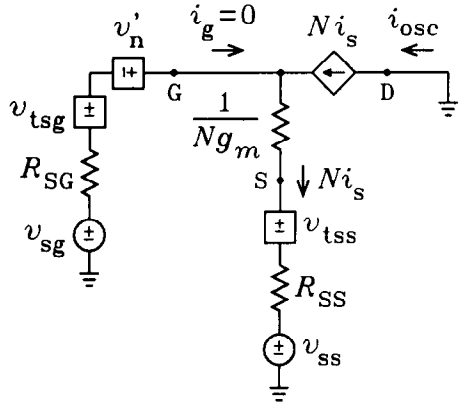

Fig. 7. Final MOSFET circuit.

T model of the MOSFET is used. The noise voltage v_n' is given by

$$v_n' = \frac{1}{N}\sum_{j=1}^{N} v_{nj} = \frac{1}{N}\sum_{j=1}^{N} \frac{i_{tdj} + i_{fdj}}{g_m}. \quad (35)$$

The following loop equation can be written for the circuit:

$$v_{sg} - v_{ss} + v_{tsg} - v_{tss} + v_n' = Ni_s\left(\frac{1}{Ng_m} + R_{SS}\right). \quad (36)$$

This equation can be solved for Ni_s to obtain

$$Ni_s = \frac{v_{sg} - v_{ss} + v_{tsg} - v_{tss} + v_n'}{1/Ng_m + R_{SS}}. \quad (37)$$

Because $i_{osc} = Ni_s$, it follows that the equivalent noise voltage in series with either v_{sg} or v_{ss} that generates the same noise in i_{osc} is given by

$$v_{ni} = v_{tsg} - v_{tss} + v_n'$$

$$= v_{tsg} - v_{tss} + \frac{1}{N}\sum_{j=1}^{N} \frac{i_{tdj} + i_{fdj}}{g_m}. \quad (38)$$

This can be converted into a mean-square voltage to obtain

$$\overline{v_{ni}^2} = 4kT(R_{SG} + R_{SS})\Delta f + \frac{4kT\Delta f}{3}\sqrt{\frac{2L}{\mu_0 C_{ox}(NW)(NI_D)}} + \frac{K_f \Delta f}{2\mu_0 C_{ox}(NW)fL}. \quad (39)$$

The first term in Eq. (39) arises from the thermal noise generated by R_{SG} and R_{SS}. The second arises from the thermal noise generated in the channel. The third term arises from the flicker noise generated in the channel. The SNR is given by Eq. (18), where $\overline{v_s^2} = \overline{v_{sg}^2}$ for the CS configuration and $\overline{v_s^2}$ and $\overline{v_{ss}^2}$ for the CG configuration. The SNR is maximized when $\overline{v_{ni}^2}$ is minimized.

2.1 Constant Stage Current

It can be seen from Eq. (39) that $\overline{v_{ni}^2}$ is a monotonically decreasing function of both N and I_D. Thus there is no optimum value for either which minimizes the noise. If the total bias current in the stage is held constant, the bias current per device is proportional to $1/N$. In this case, NI_D is a constant and $\overline{v_{ni}^2}$ is a function of the product NW. The thermal noise component decreases by 1.5 dB each time N is doubled while the flicker noise component decreases by 3 dB.

Because $\overline{v_{ni}^2}$ is a function of NW, it follows that increasing the width of a single device by a factor N has the same effect on the noise as connecting N devices in parallel. However, this conclusion must be considered to be an oversimplification due to the limitations of physical devices. For example, it ignores the issue of the effective series gate resistance. The resistance of the physically long and narrow polysilicon gate in a wide-gate device can be significant. While the effective gate resistance is reduced by a factor of N when N devices are paralleled, this is not necessarily true for a single device of N times the width. In addition, the high-frequency response of the latter device is degraded by the distributed delay line formed by the gate resistance and capacitance.

2.2 Constant Device Current

If $R_{SG} = R_{SS} = 0$ and I_D is held constant, the total bias current in the stage is proportional to N. For this case, it follows from Eq. (39) that $\overline{v_{ni}^2} \propto 1/N$. Thus the noise is reduced by 3 dB each time N is doubled. For $R_{SG} > 0$ or $R_{SS} > 0$, the thermal and flicker noise components both decrease by 3 dB each time N is doubled. However, the total noise decreases by less than 3 dB because the thermal noise generated by R_{SG} and R_{SS} is not a function of N. As with the BJT stage, the power dissipation increases as N^2.

3 CONCLUSIONS

The noise performance of an amplifier stage that consists of a number of devices in parallel is a function of both the number of devices and the total bias current of the stage. If the total bias current is held constant as the number of devices is varied, the noise varies differently than if the bias current per device is held constant. These effects have been investigated here for the BJT and the MOSFET. For a constant total bias current it has been shown that the parallel connection of BJTs can only be used to decrease the noise generated by the BJT base spreading resistance. The decrease in noise achieved by the parallel connection of MOSFETs can be achieved by fabricating a single MOSFET with an effective gate width that is larger by a factor equal to the number of parallel devices.

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